Fig.1 (Prior Art)

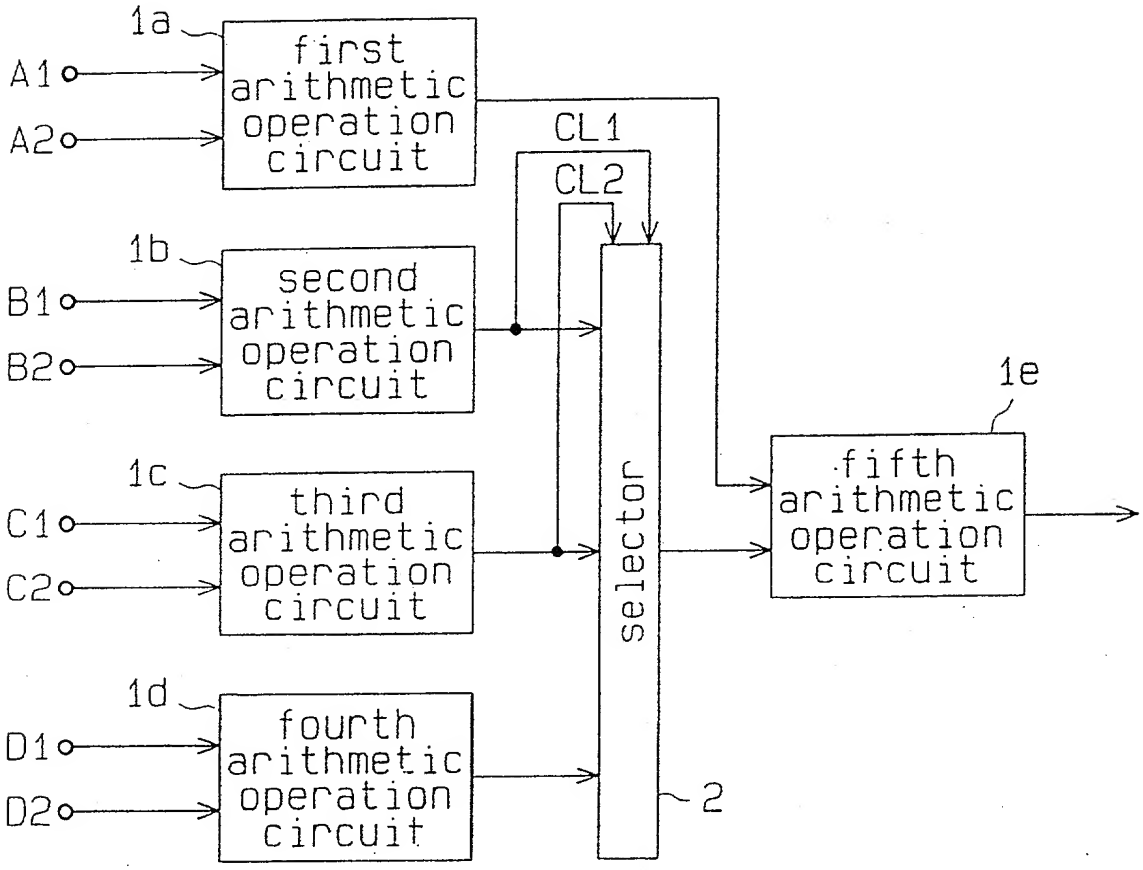


Fig.2

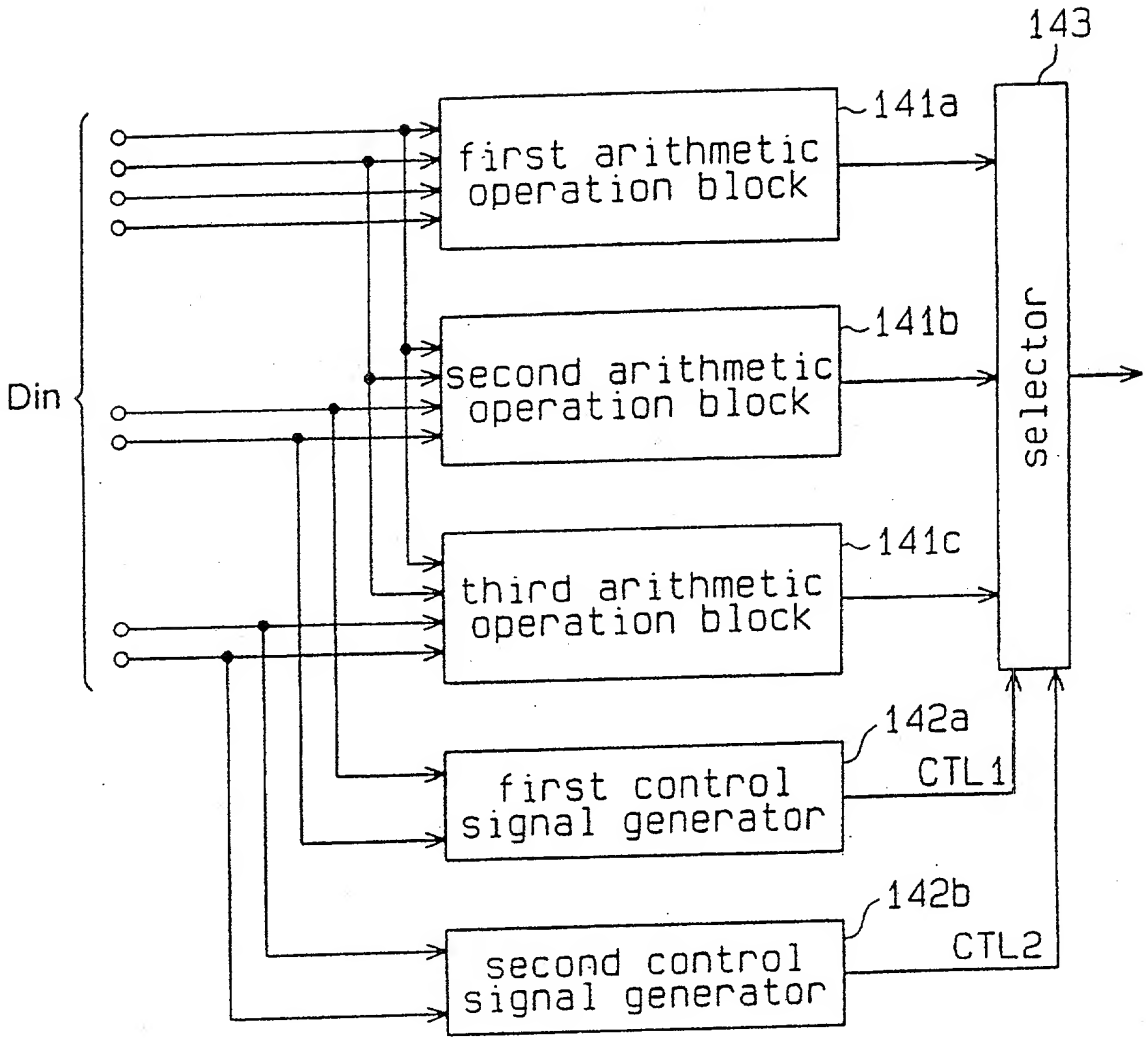

143
141a
first arithmetic operation block
141b
second arithmetic operation block
141c
third arithmetic operation block
selector
Din
142a
CTL1
first control signal generator
142b
CTL2
second control signal generator

Fig.3

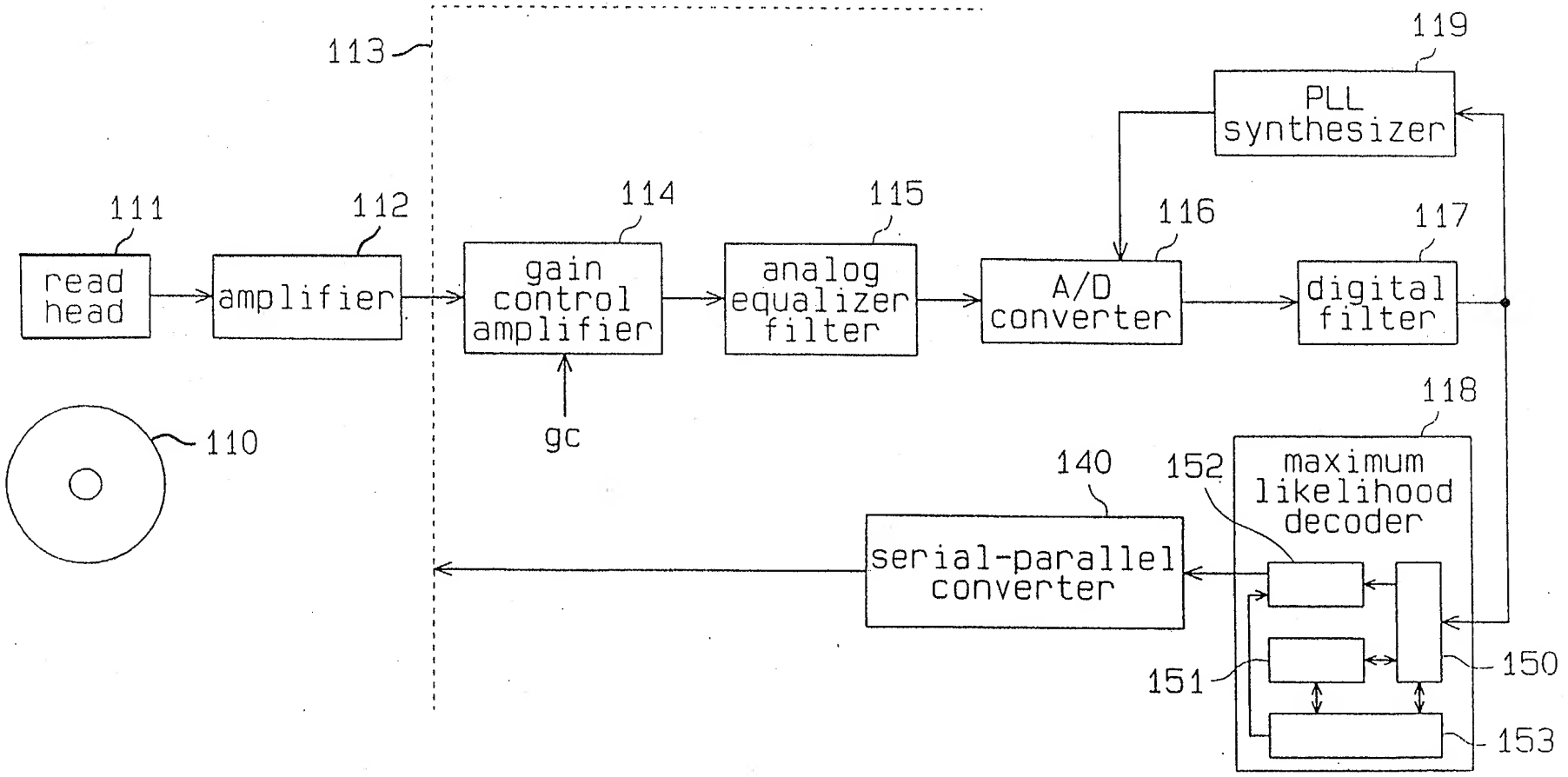


Fig.4

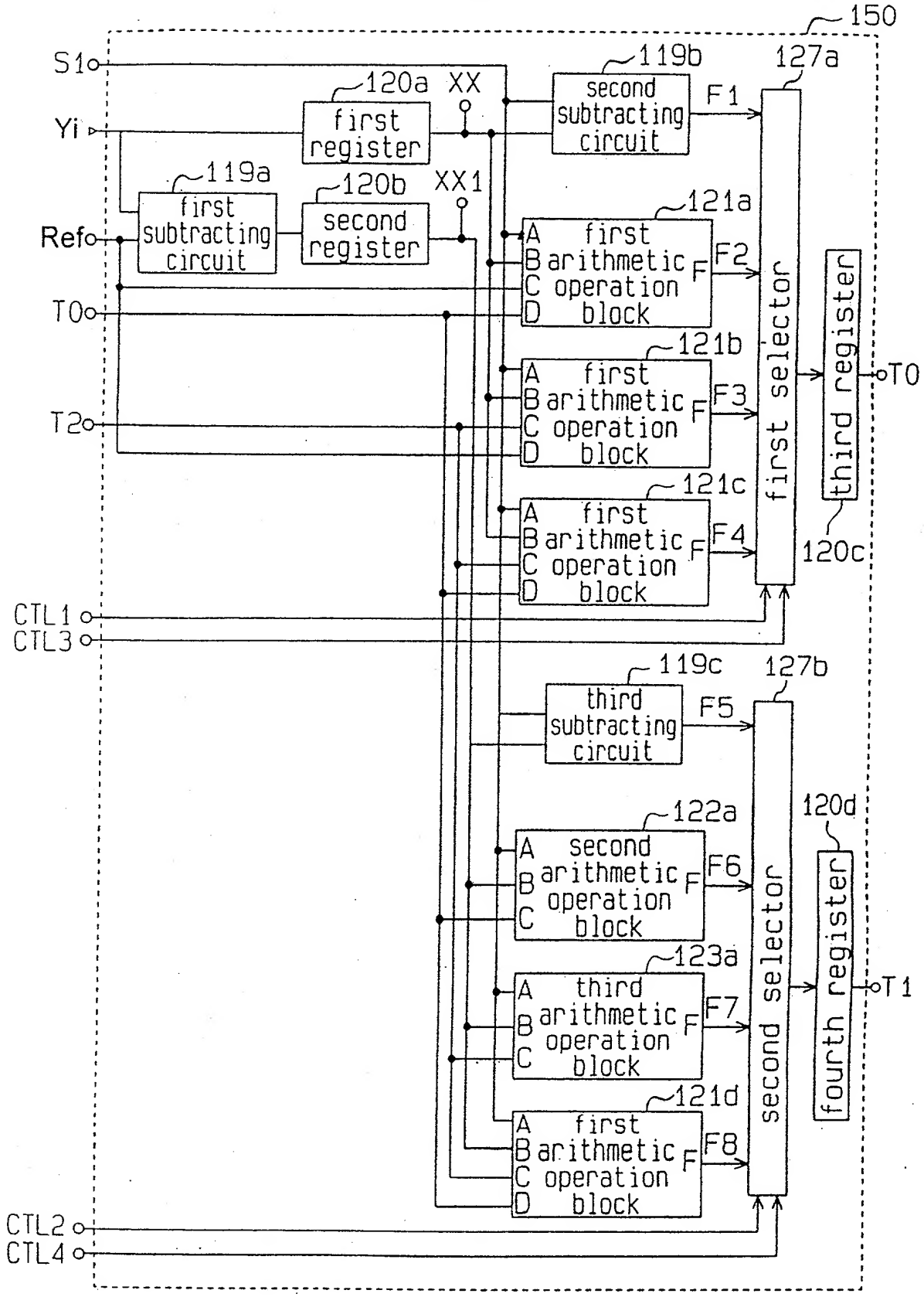

150
S1
Yi
Refo
T0
T2
CTL1
CTL3
CTL2
CTL4
119a
first subtracting circuit
120a
first register
XX
120b
second register
XX1
119b
second subtracting circuit
F1
127a
first selector
121a
A first
B arithmetic
C operation
D block
F
F2
121b
F3
121c
F4
third register
T0
120c
119c
third subtracting circuit
F5
127b
second selector
122a
second arithmetic operation block
F6
123a
third arithmetic operation block
F7
121d
F8
120d
fourth register
T1

Fig.5

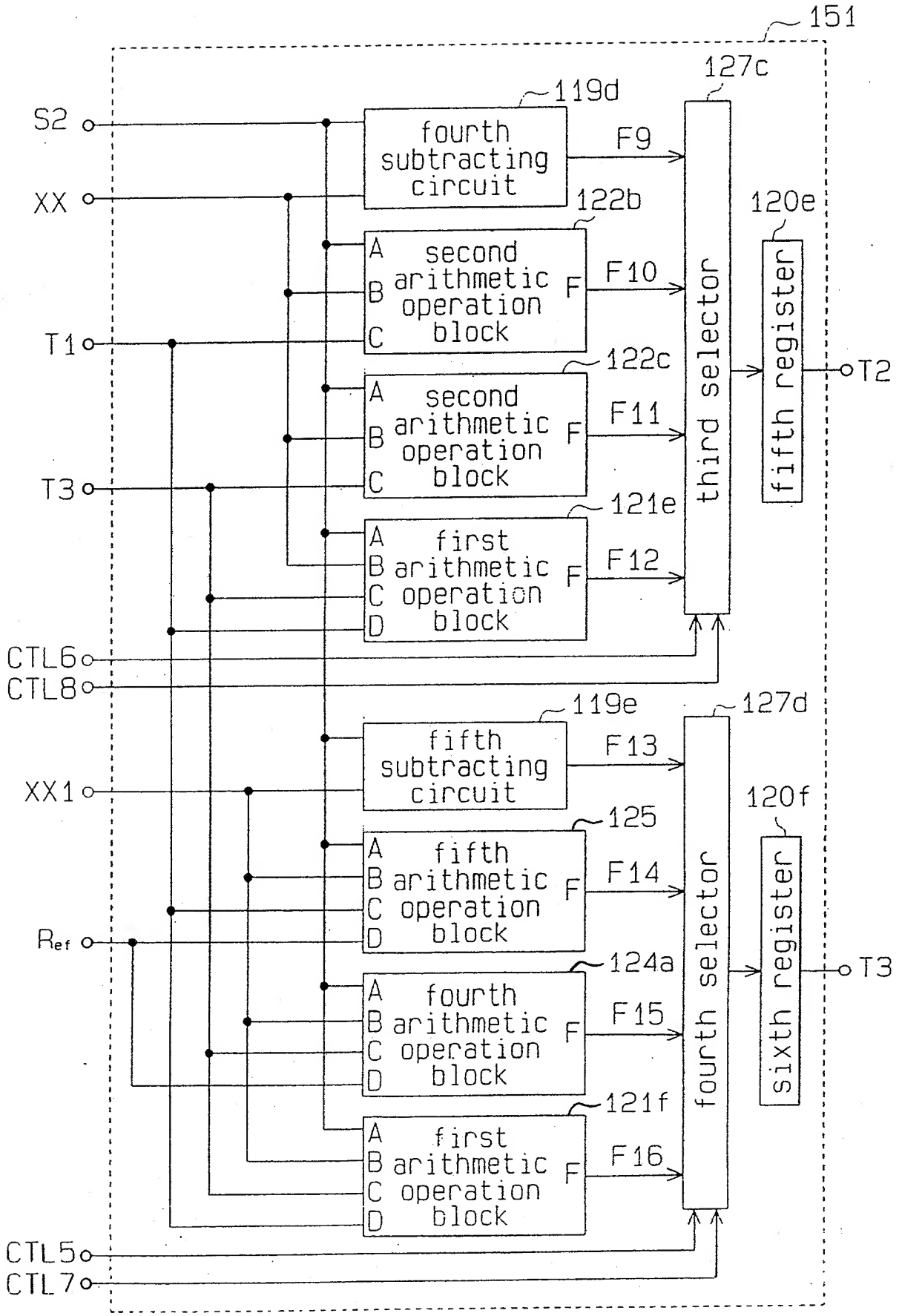

151
127c
119d
S2
XX
fourth subtracting circuit
F9
122b
120e
A
B
C
second arithmetic operation block
F
F10
fifth register
T1
122c
T2
T3
F11
121e
first arithmetic operation block
F12
third selector
CTL6
CTL8
119e
127d
fifth subtracting circuit
F13
XX1
120f
125
fifth arithmetic operation block
F14
Ref
124a
T3
fourth arithmetic operation block
F15
fourth selector
sixth register
121f
first arithmetic operation block
F16
CTL5
CTL7

Fig.6

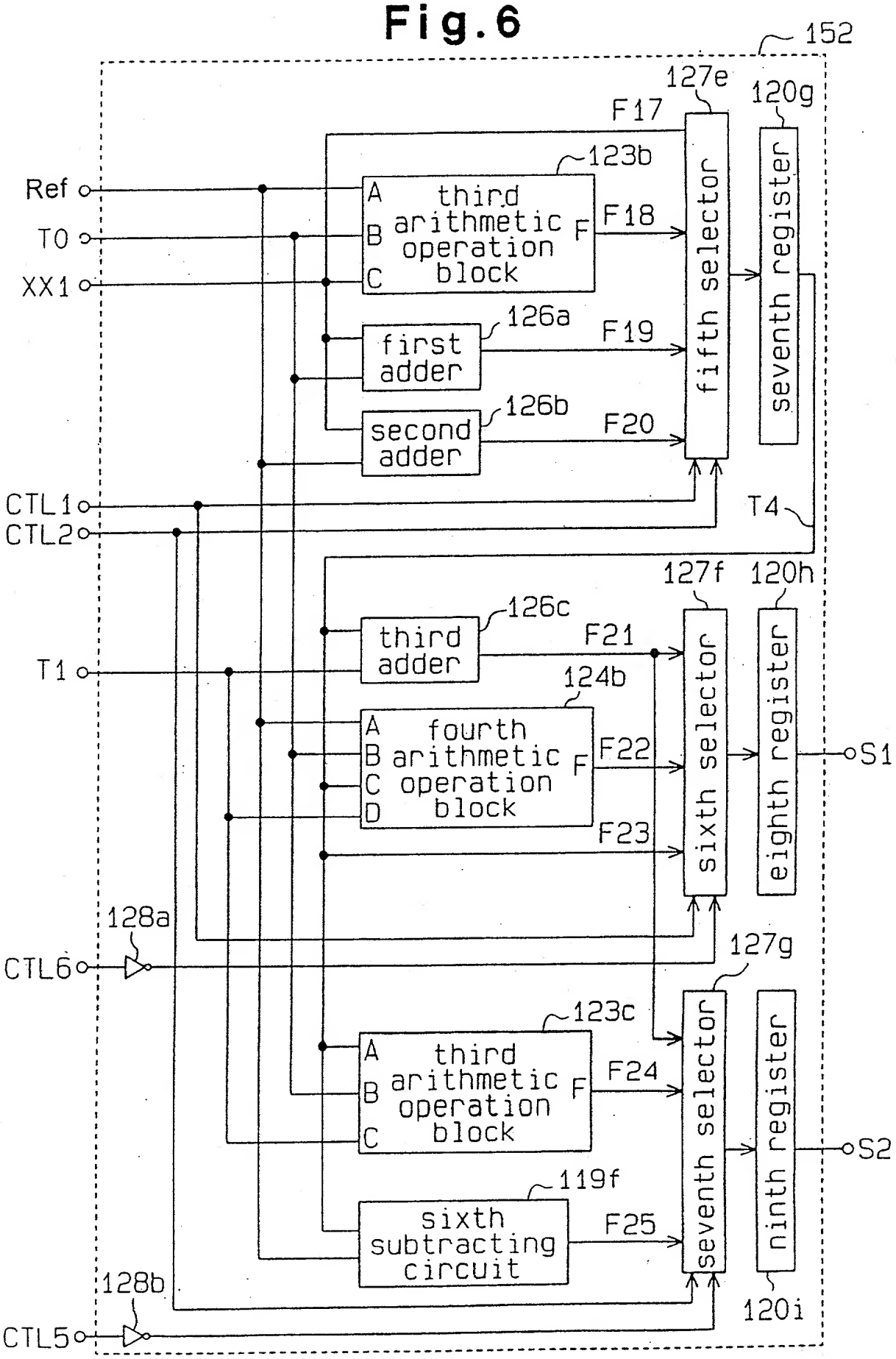

152
127e
120g
F17
123b
Ref
T0
XX1
A
B
C
third arithmetic operation block
F
F18
126a
first adder
F19
126b
second adder
F20
fifth selector
seventh register
CTL1
CTL2
T4
127f
120h
126c
third adder
F21
T1
124b
A
B
C
D
fourth arithmetic operation block
F
F22
F23
sixth selector
eighth register
S1
128a
CTL6
127g
123c
third arithmetic operation block
F24
119f
sixth subtracting circuit
F25
seventh selector
ninth register
S2
128b
CTL5
120i

Fig.7

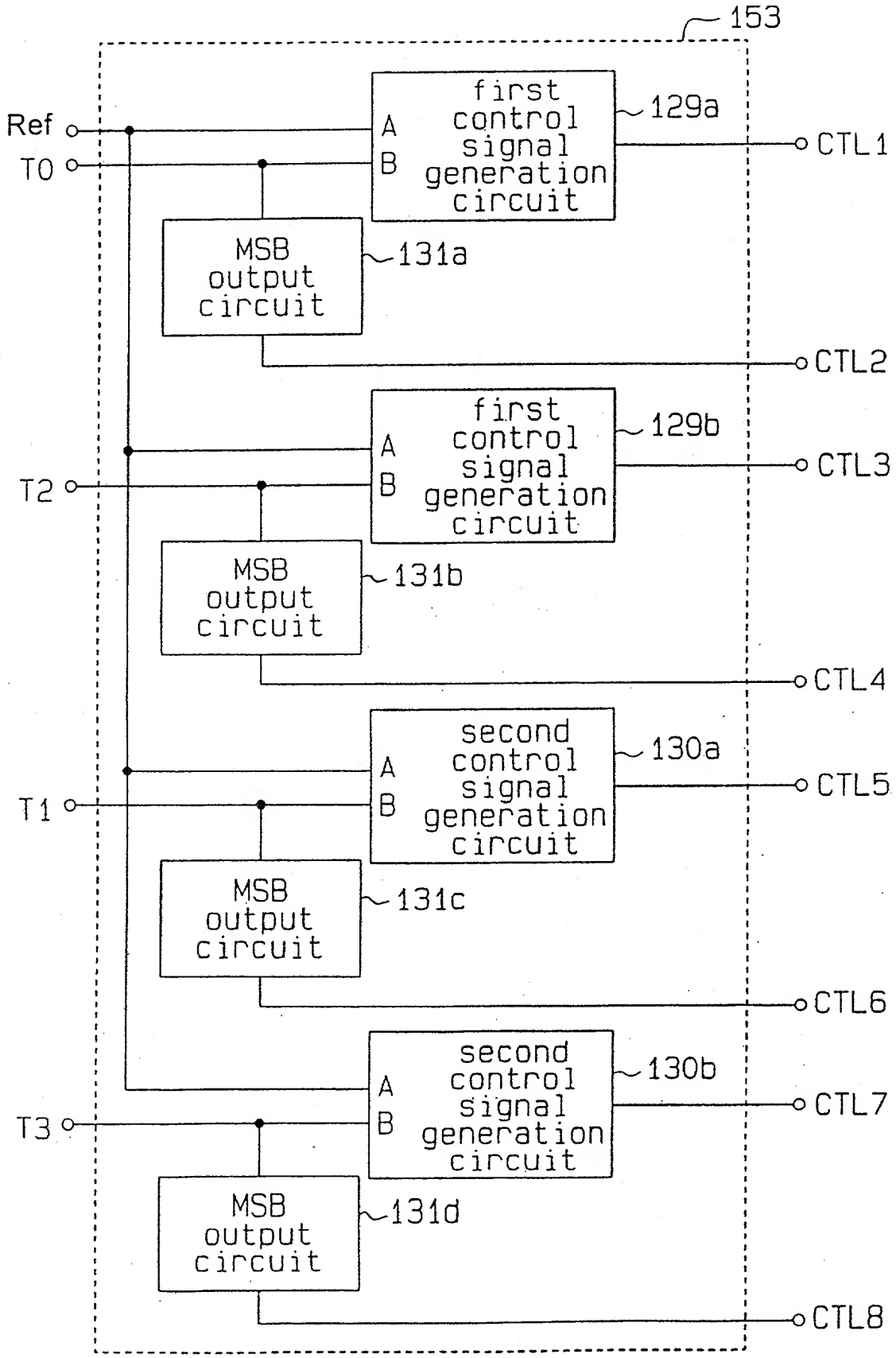
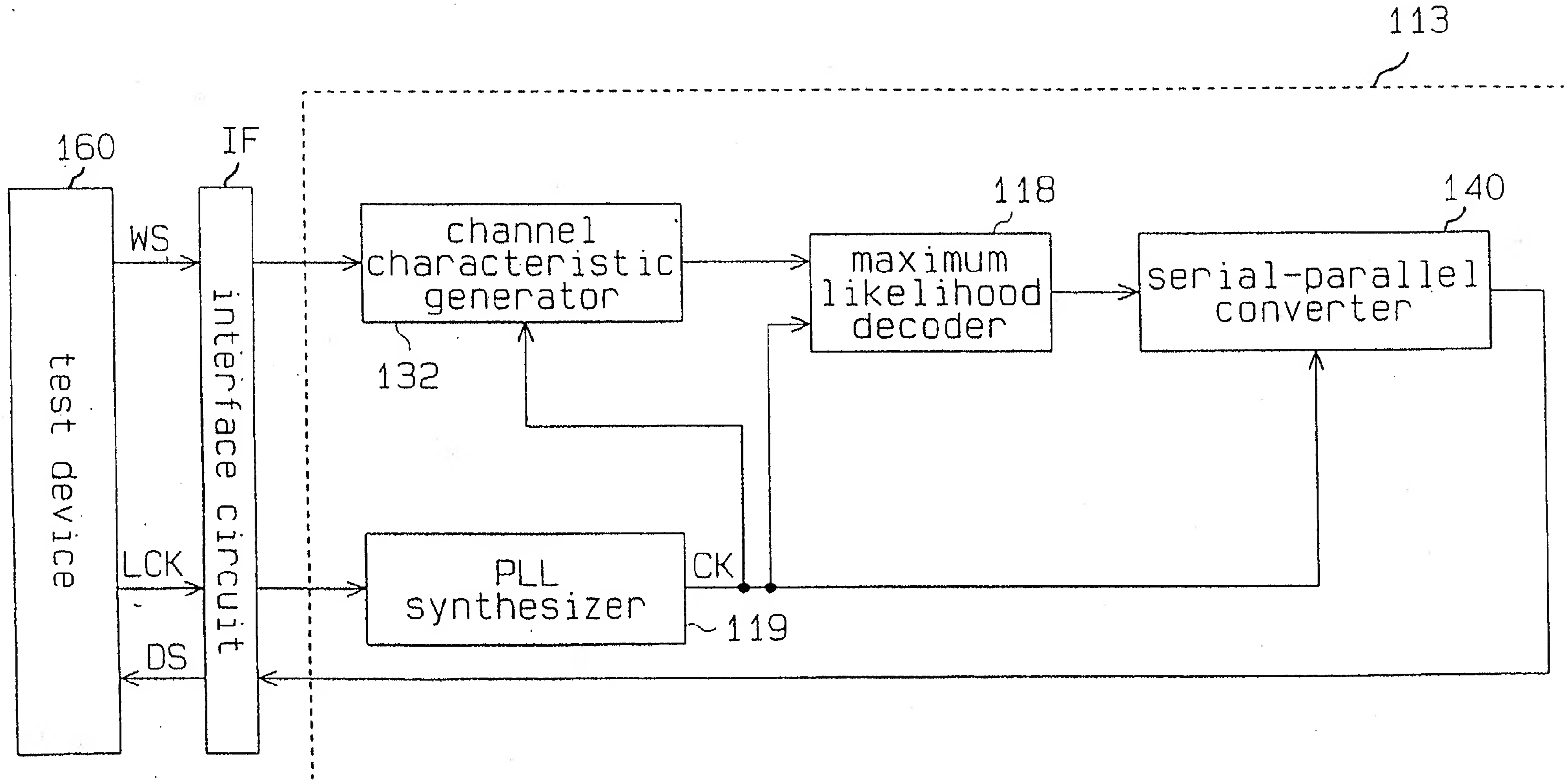

153
Ref
T0
T1
T2
T3
A
B
first control signal generation circuit
129a
second control signal generation circuit
130a
130b
MSB output circuit
131a
131b
131c
131d
CTL1
CTL2
CTL3
CTL4
CTL5
CTL6
CTL7
CTL8

Fig.8



113
160
IF
test device
interface circuit
WS
LCK
DS
channel characteristic generator
132
PLL synthesizer
119
CK
maximum likelihood decoder
118
serial-parallel converter
140

Fig.9

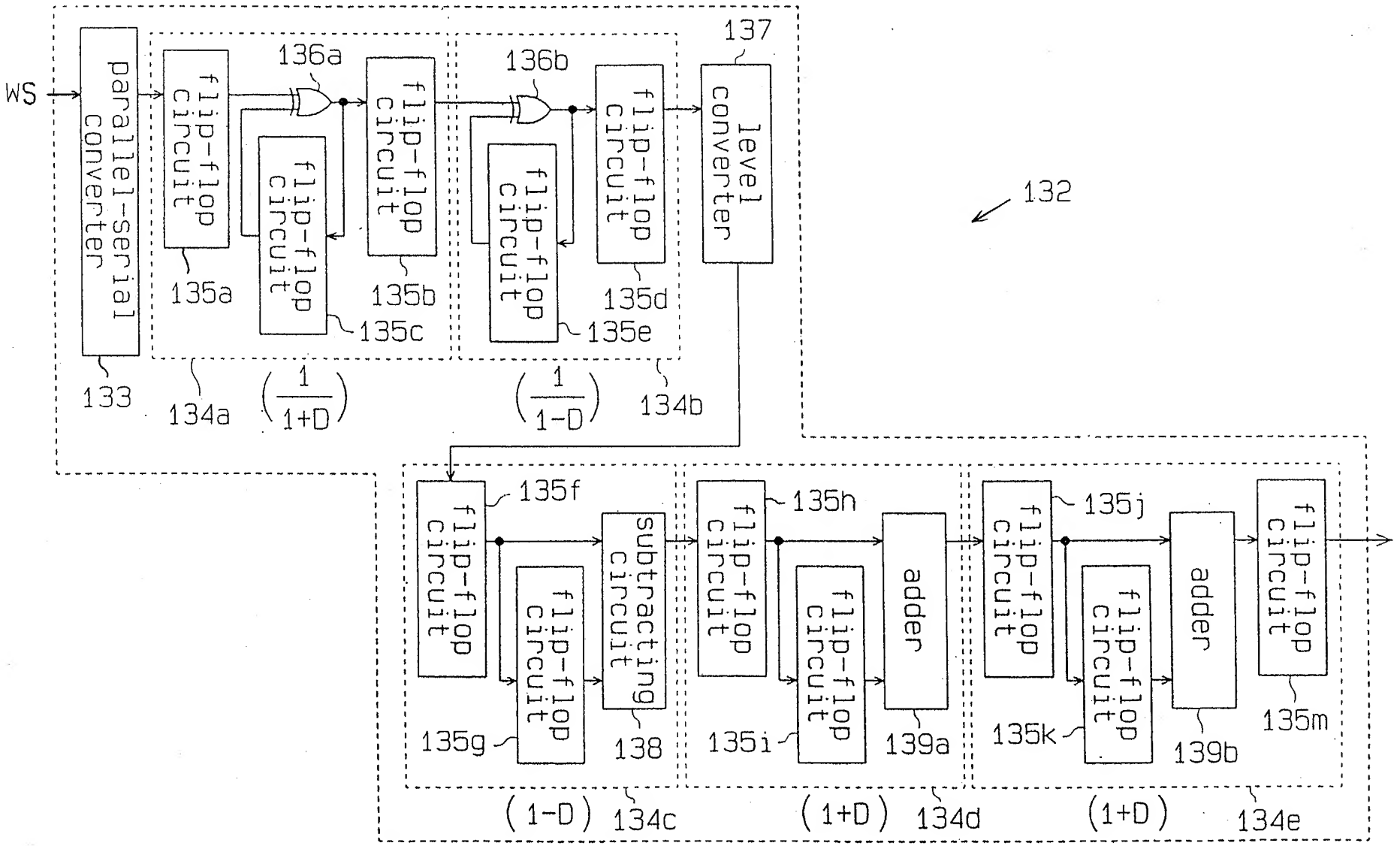


Fig.10

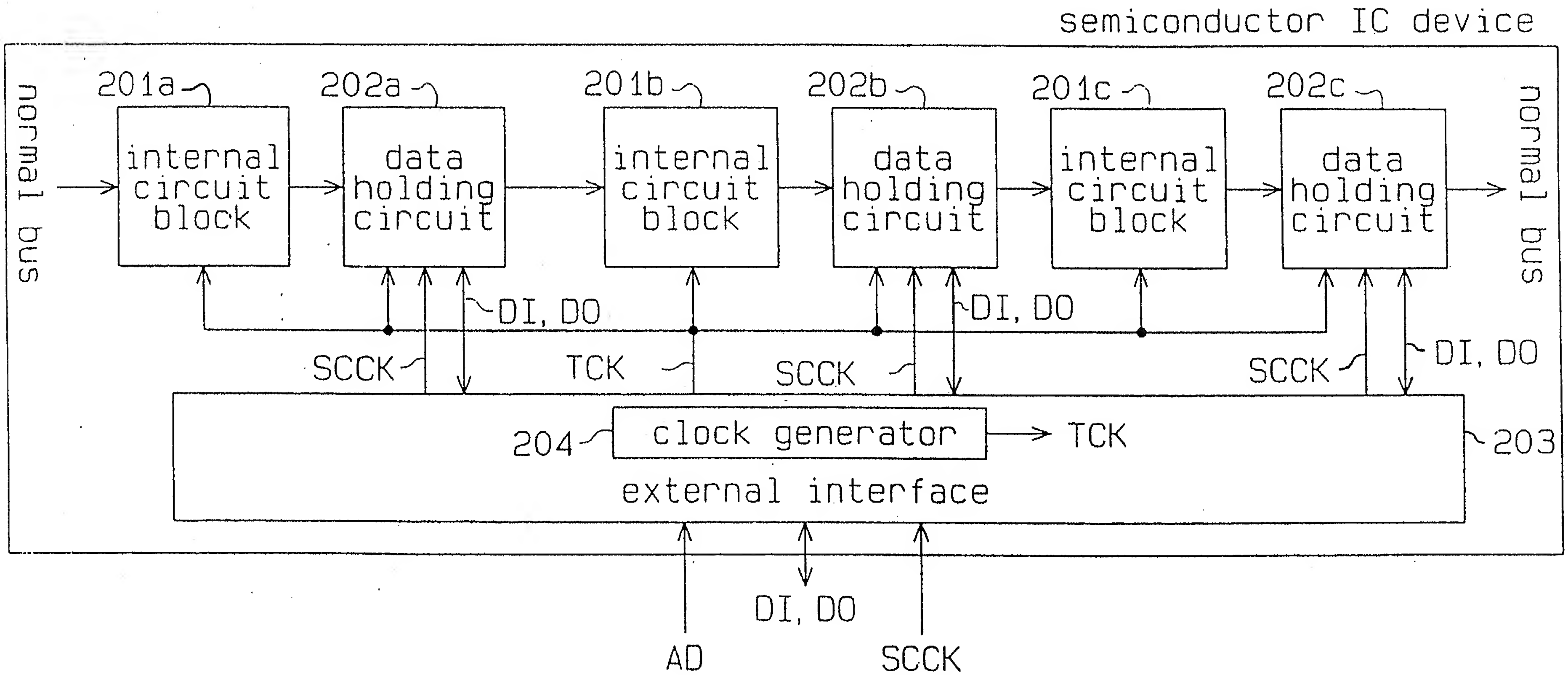

semiconductor IC device
normal bus
201a
internal circuit block
202a
data holding circuit
201b
internal circuit block
202b
data holding circuit
201c
internal circuit block
202c
data holding circuit
normal bus
DI, DO
SCCK
TCK
SCCK
DI, DO
SCCK
DI, DO
204
clock generator
TCK
203
external interface
AD
DI, DO
SCCK

Fig.11

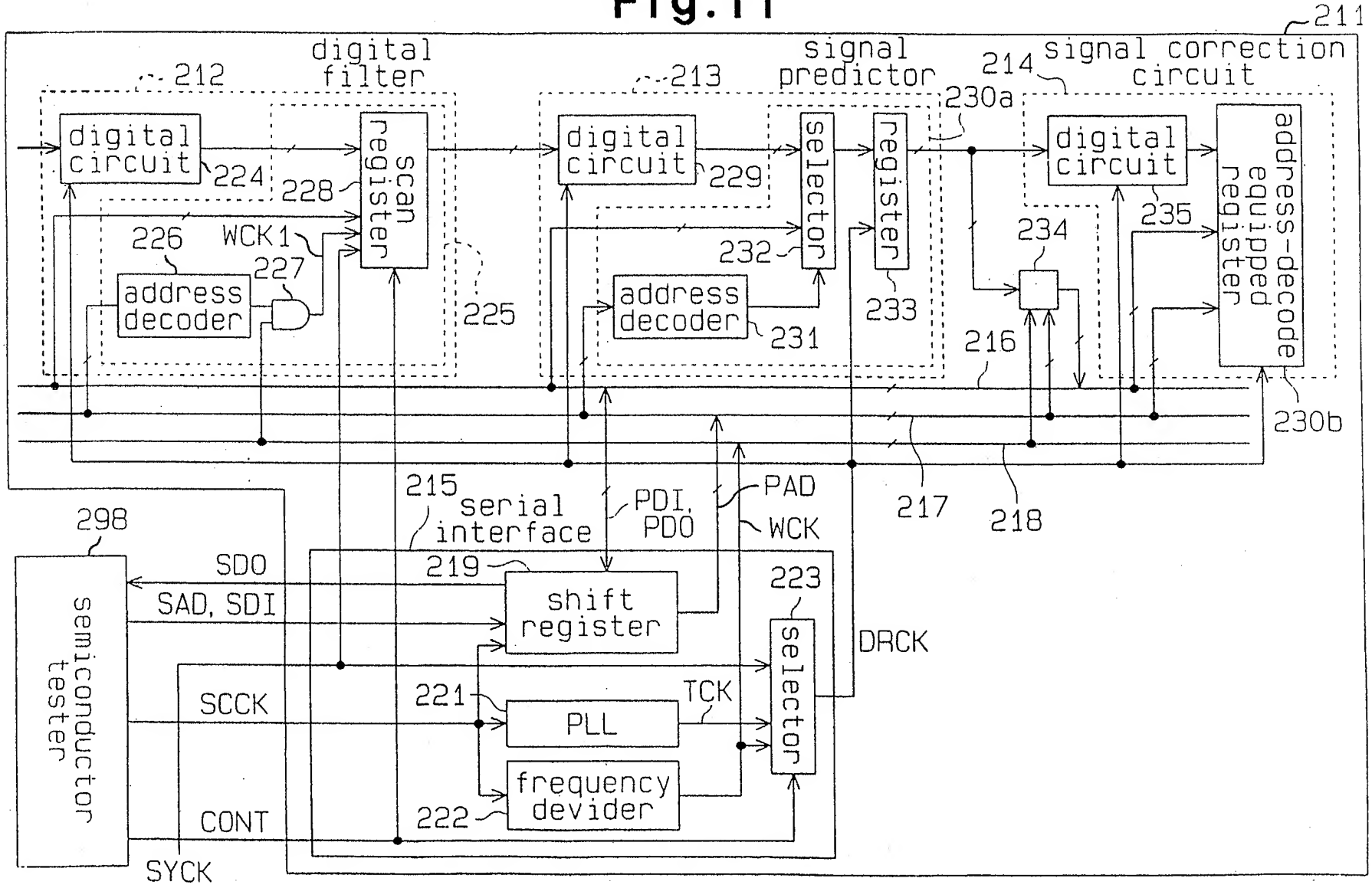

211
212
digital filter
213
signal predictor
214
signal correction circuit
digital circuit
224
228
scan register
226
WCK1
227
address decoder
225
digital circuit
229
232
selector
register
233
address decoder
231
230a
digital circuit
235
234
address-decode equipped register
230b
216
217
218
215
serial interface
PDI, PDO
PAD
WCK
298
semiconductor tester
SDO
SAD, SDI
SCCK
CONT
SYCK
219
shift register
223
selector
DRCK
221
PLL
TCK
frequency devider
222

Fig.12

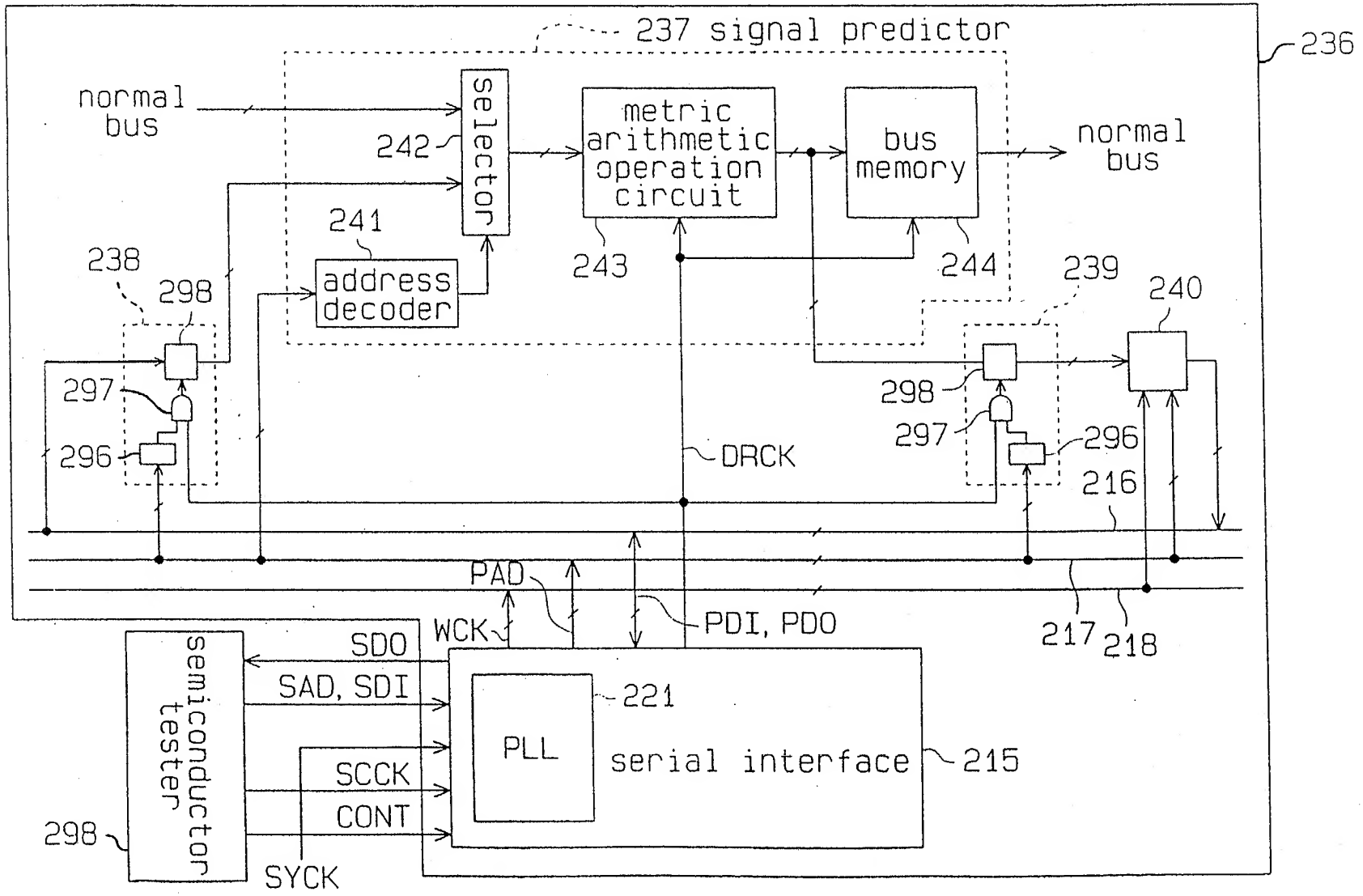


Fig.13

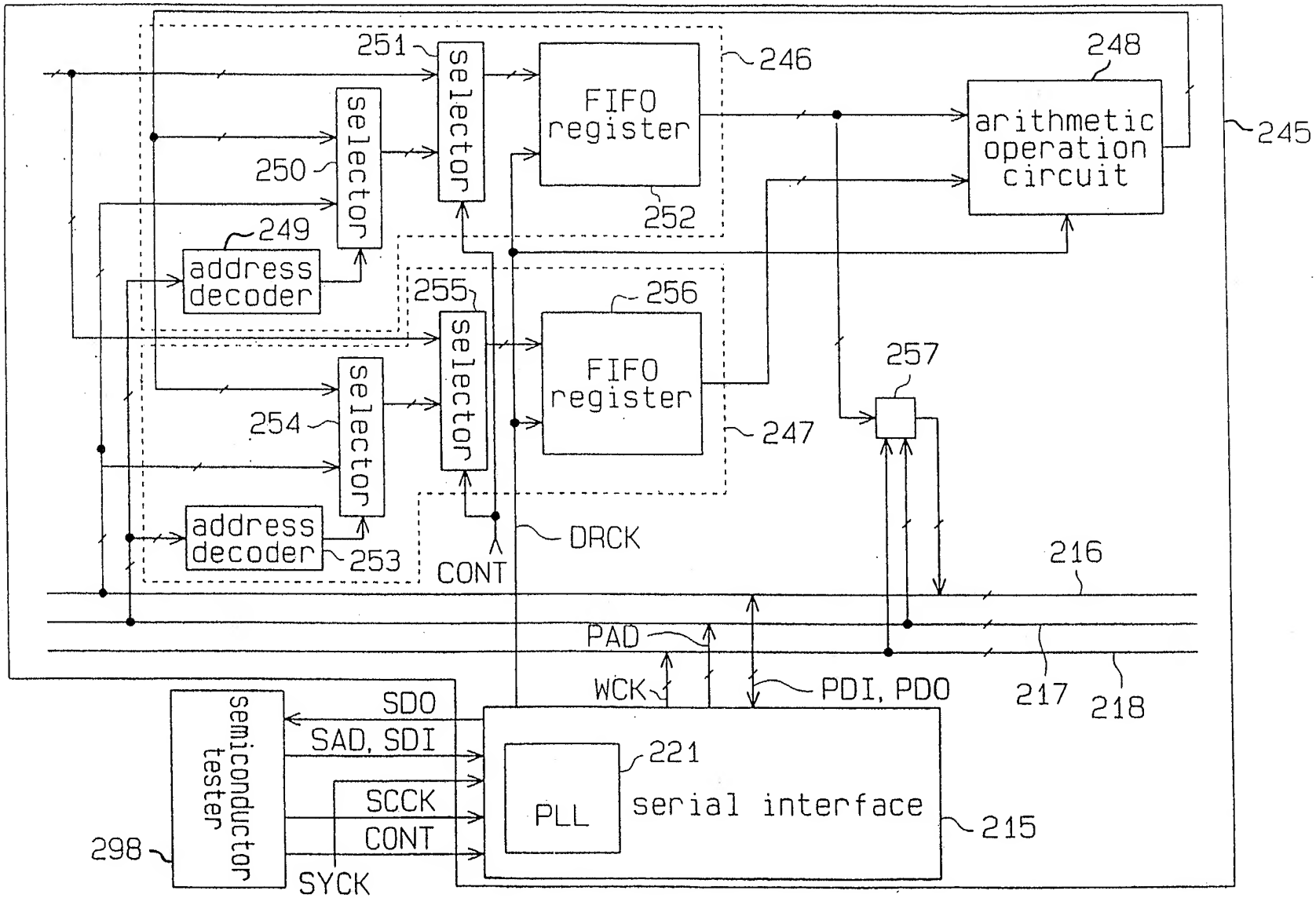

251
selector
246
FIFO register
248
arithmetic operation circuit
245
250
selector
249
address decoder
252
255
selector
256
FIFO register
257
254
selector
247
address decoder
253
CONT
DRCK
216
PAD
WCK
PDI, PDO
217
218
semiconductor tester
SDO
SAD, SDI
SCCK
CONT
SYCK
298
PLL
221
serial interface
215

Fig.14

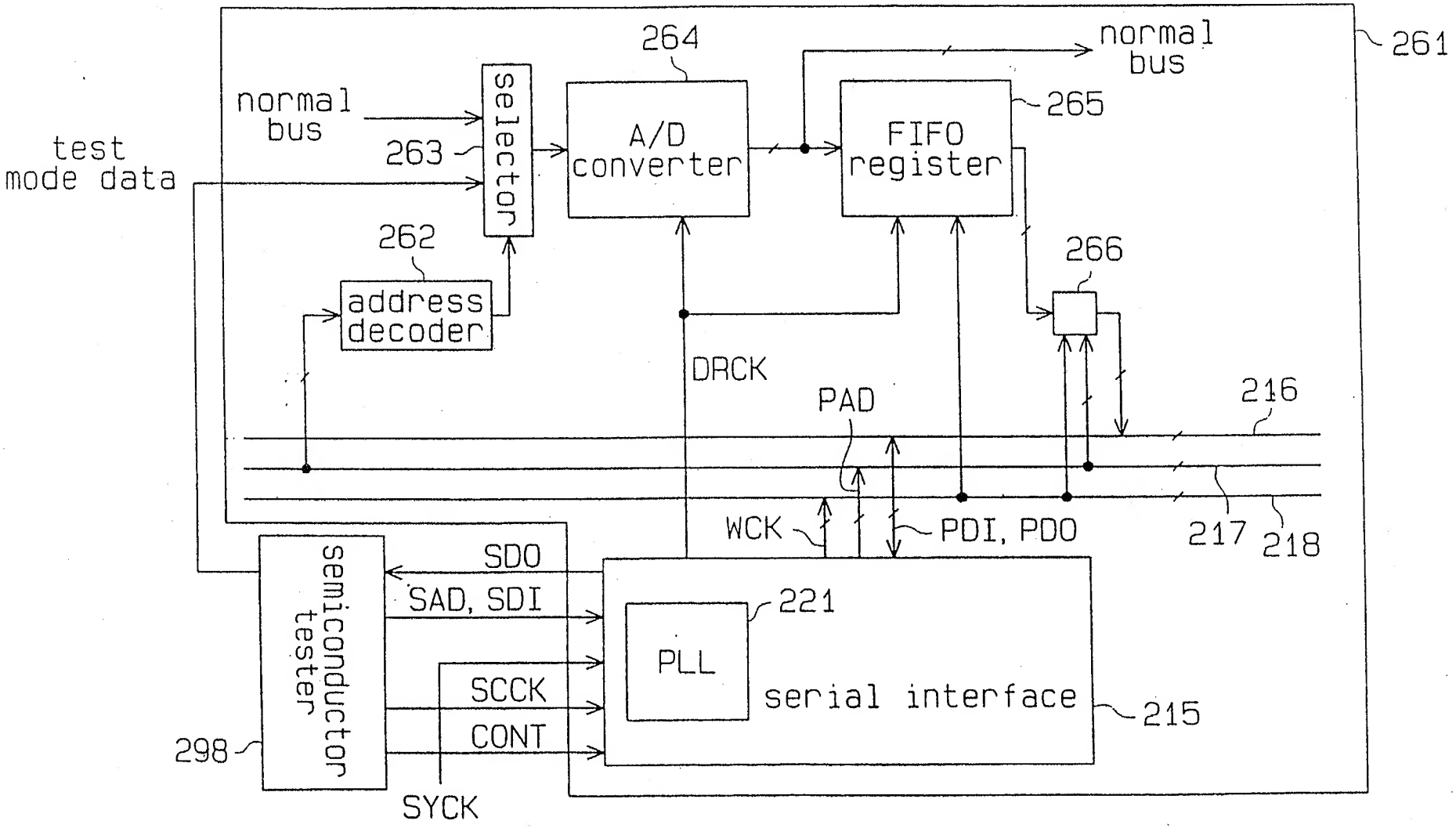

261
264
normal bus
normal bus
selector
263
A/D converter
FIFO register
265
test mode data
262
address decoder
266
DRCK
PAD
216
WCK
PDI, PDO
217
218
SDO
SAD, SDI
SCCK
CONT
SYCK
semiconductor tester
298
221
PLL
serial interface
215

Fig.15

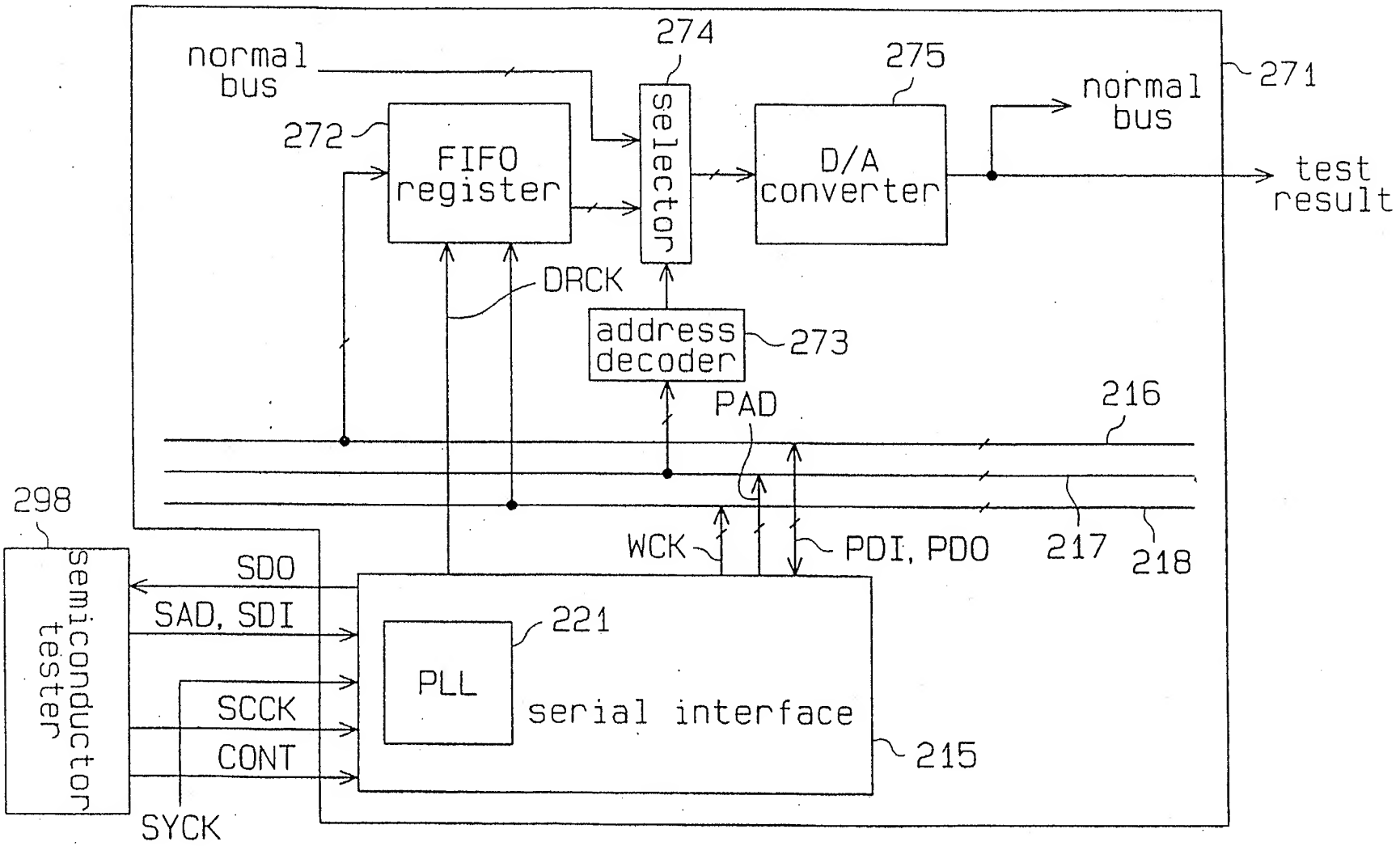


Fig.16

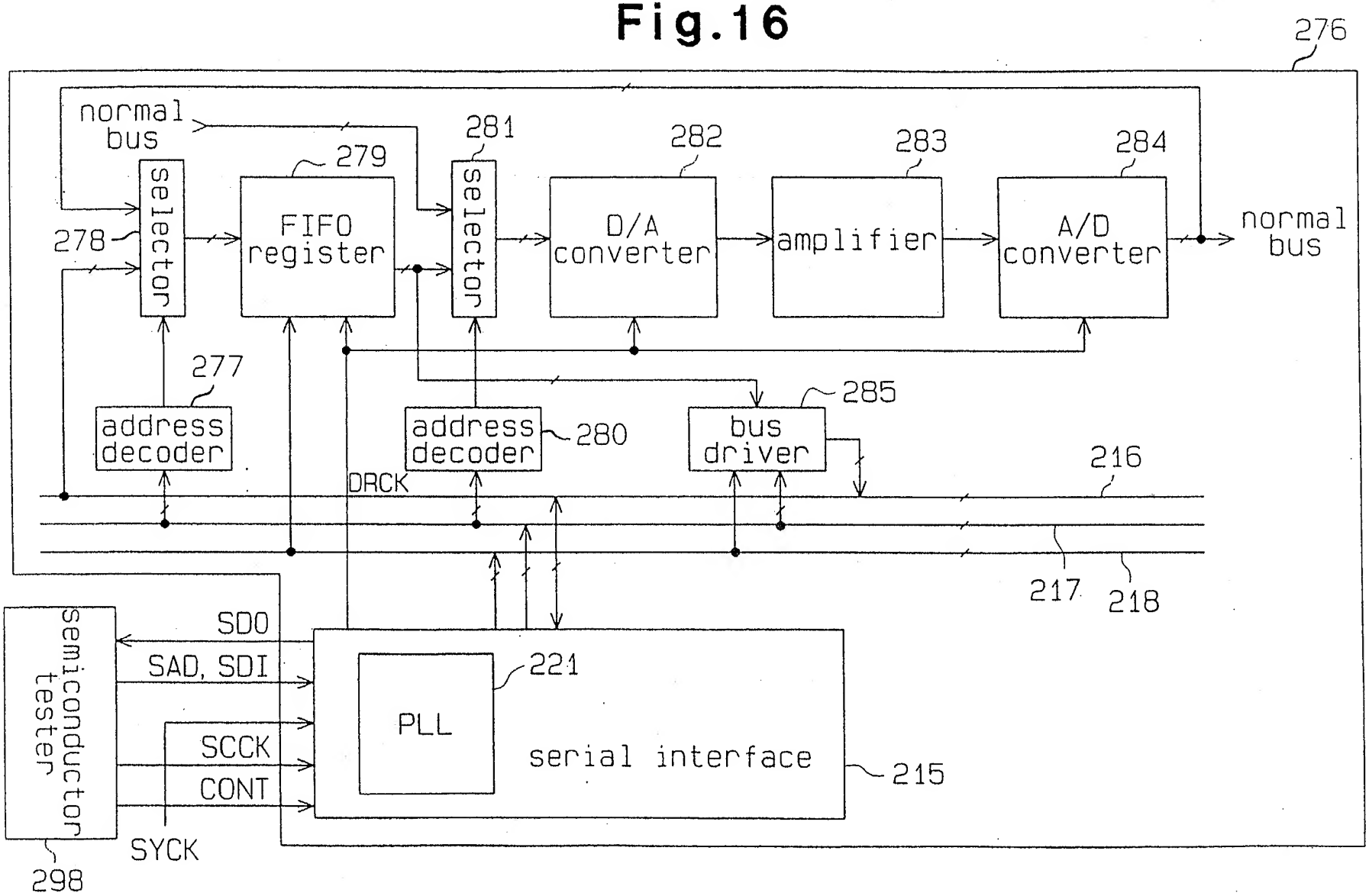


Fig.17

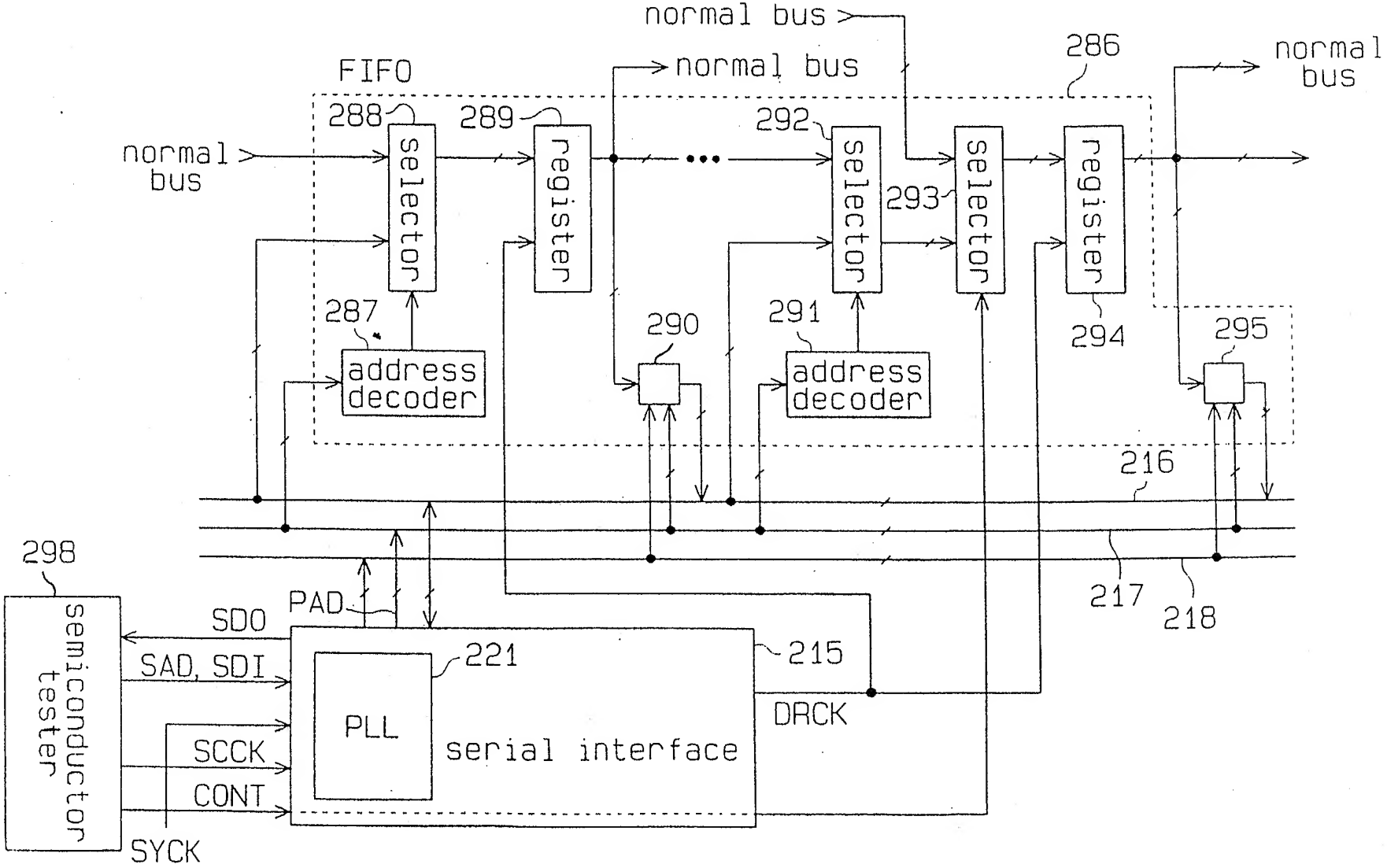


Fig.18

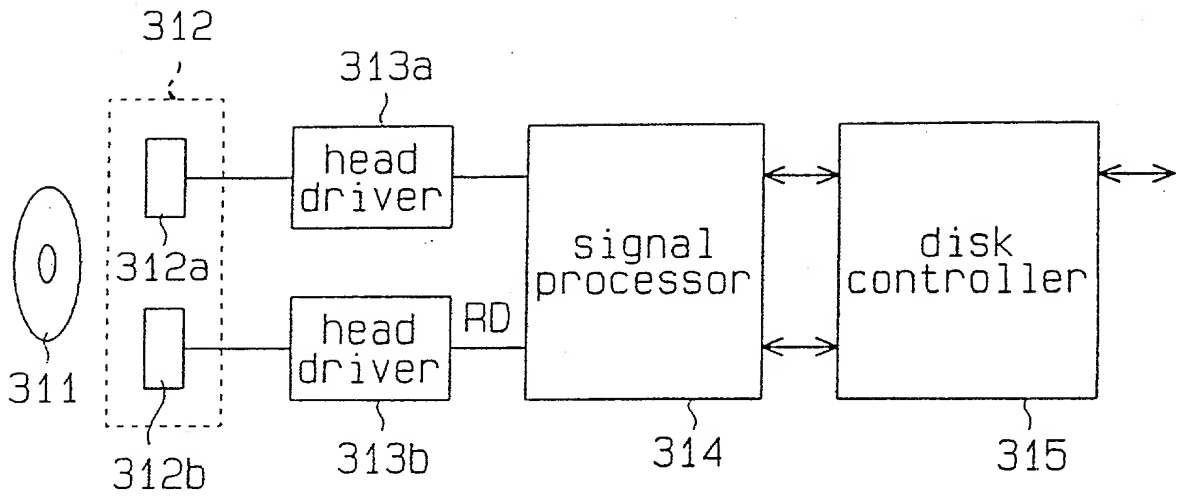

312
313a
head driver
signal processor
disk controller
312a
RD
head driver
311
312b
313b
314
315

Fig.19

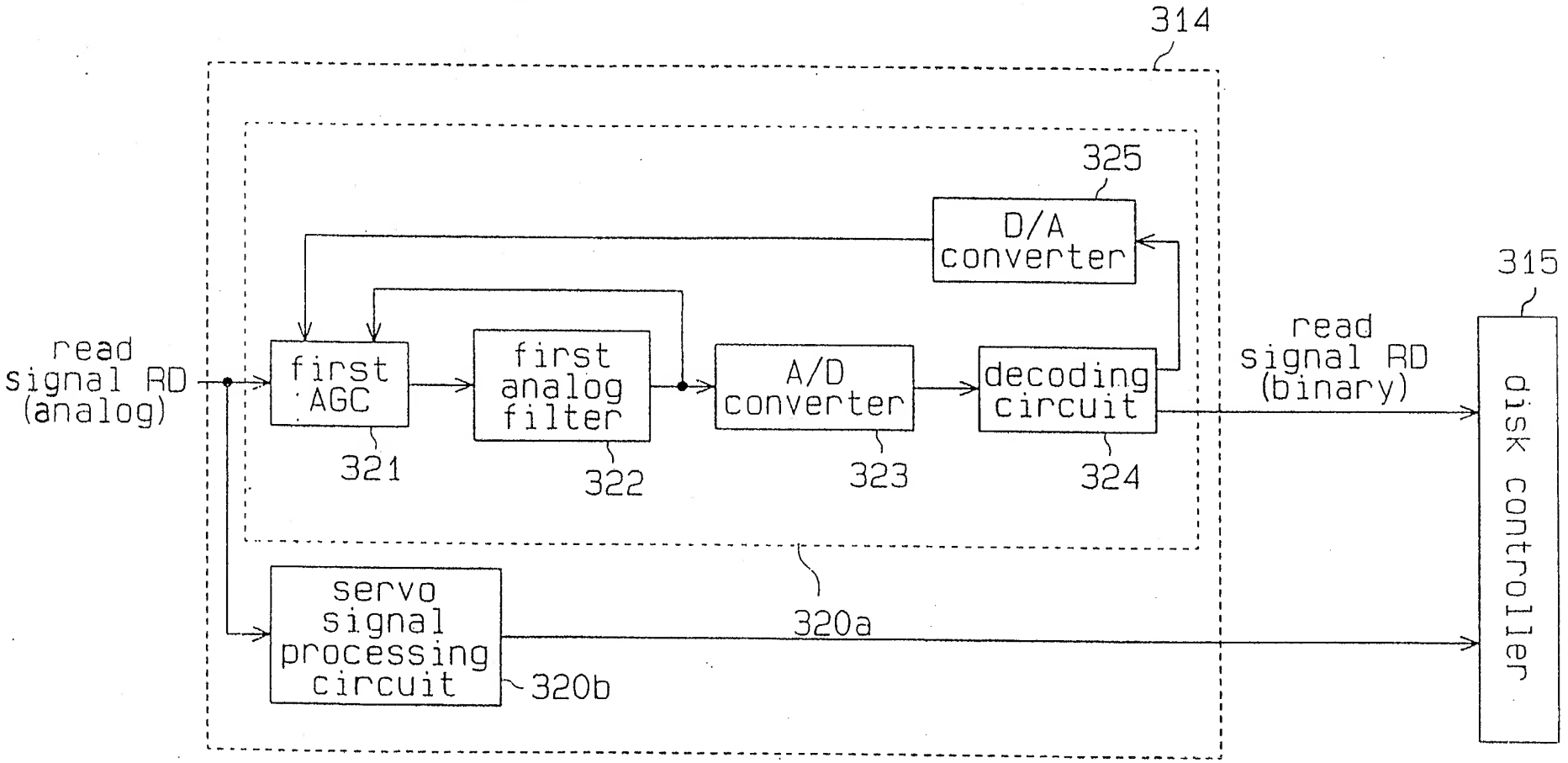


Fig.20

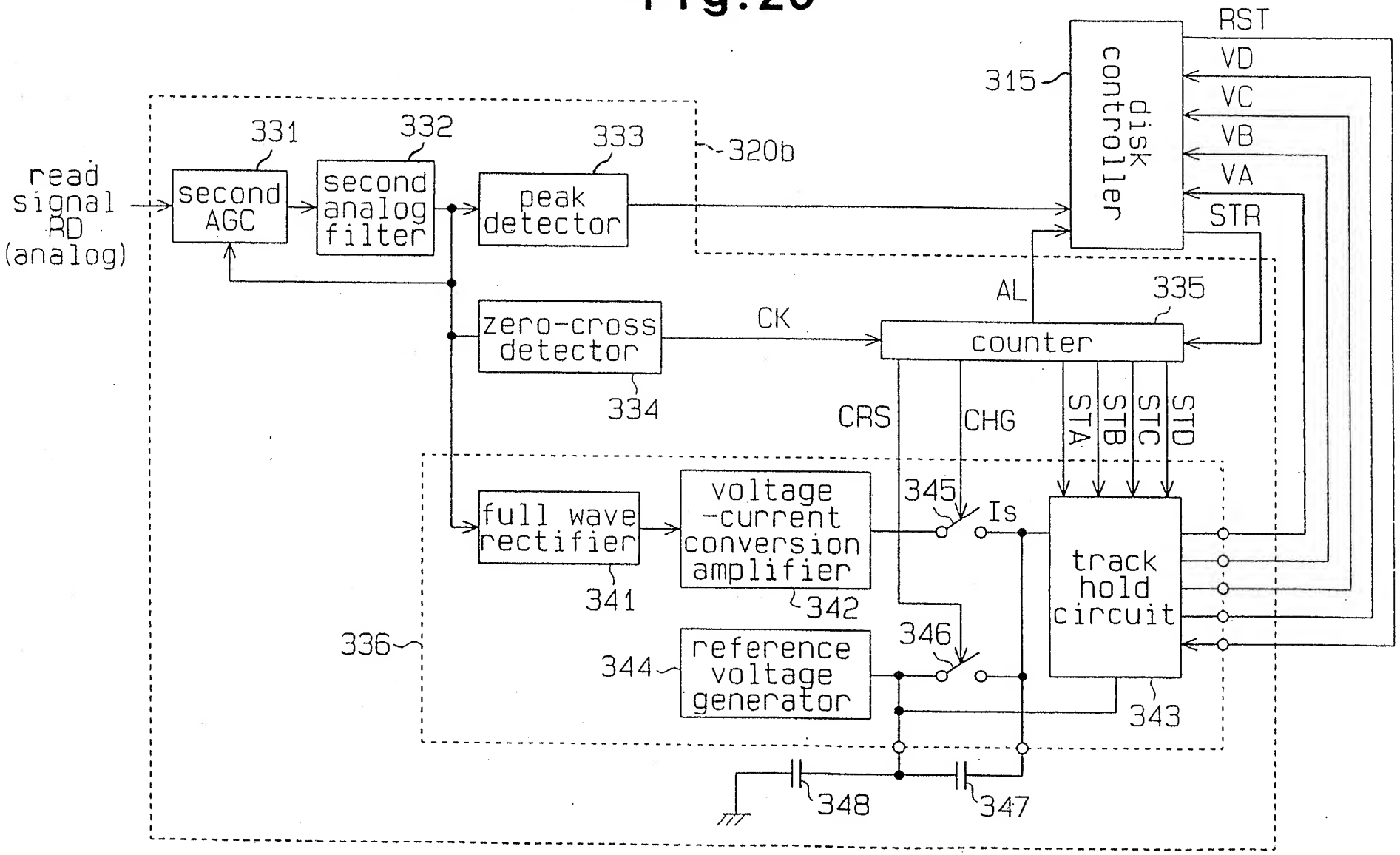


Fig.21

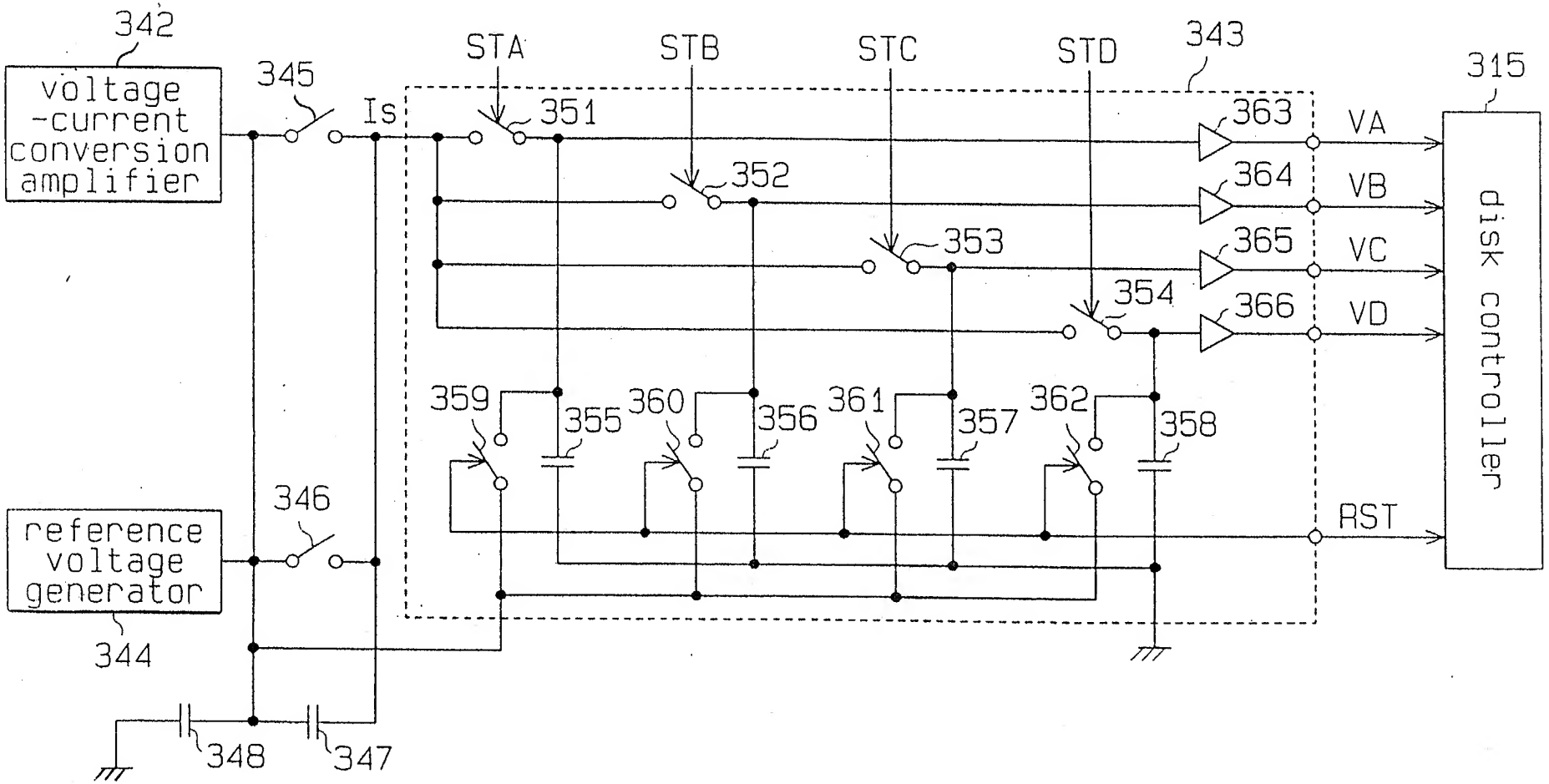

342
voltage -current conversion amplifier
345
Is
STA
STB
STC
STD
343
315
351
352
353
354
363
364
365
366
VA
VB
VC
VD
disk controller
359
355
360
356
361
357
362
358
RST
346
reference voltage generator
344
348
347

Fig.22

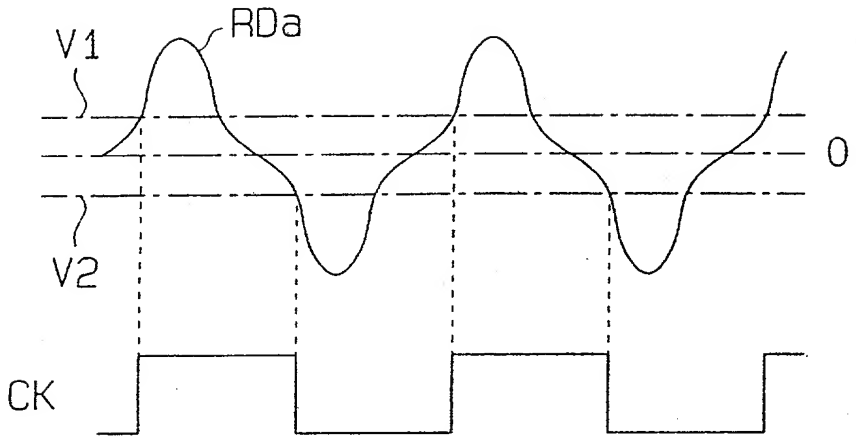


Fig.23

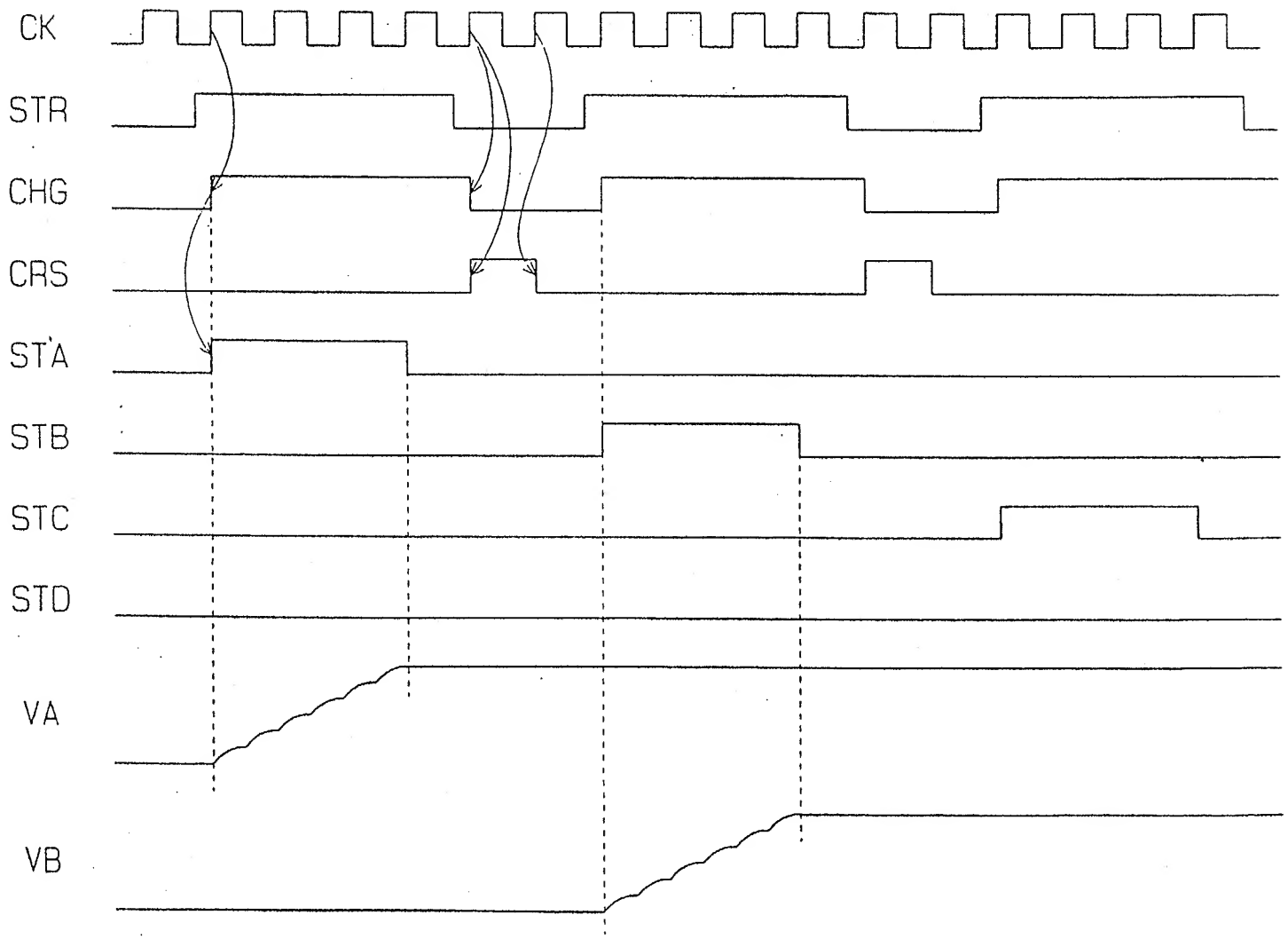


Fig.24

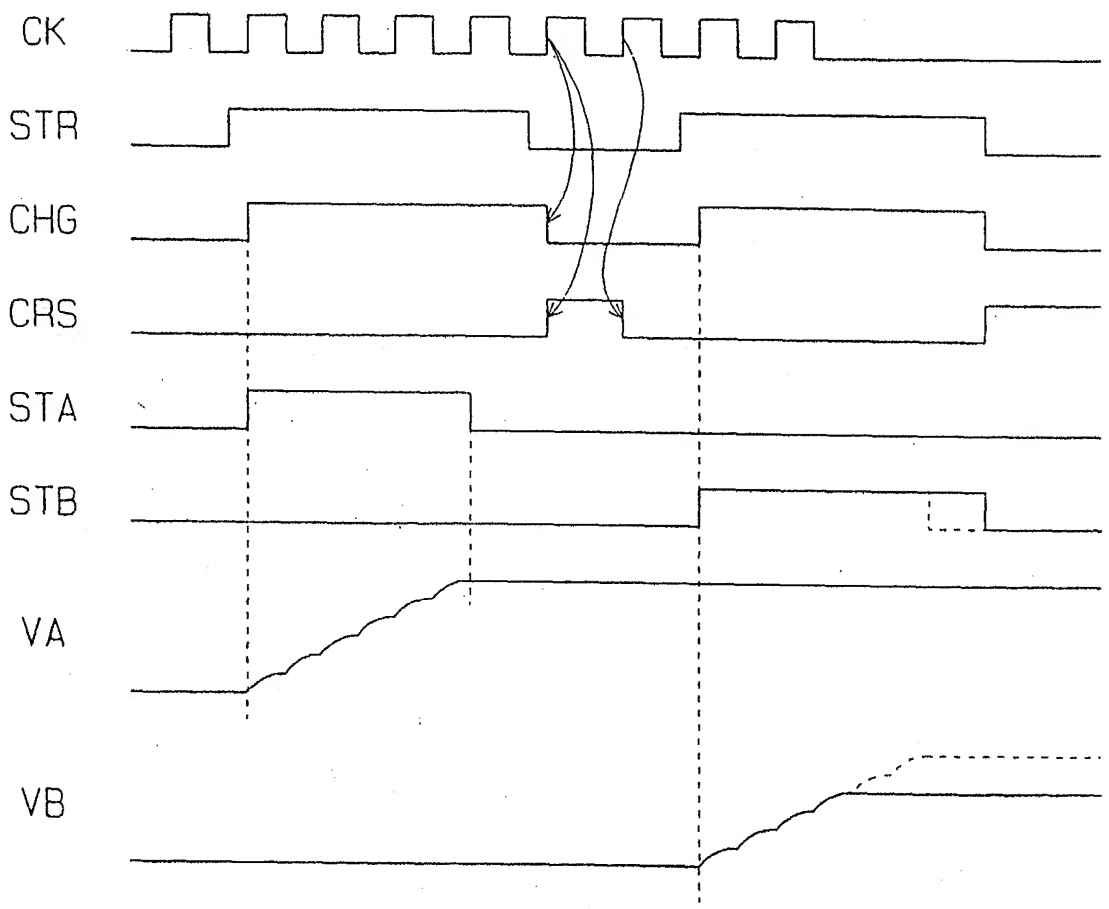


Fig.25

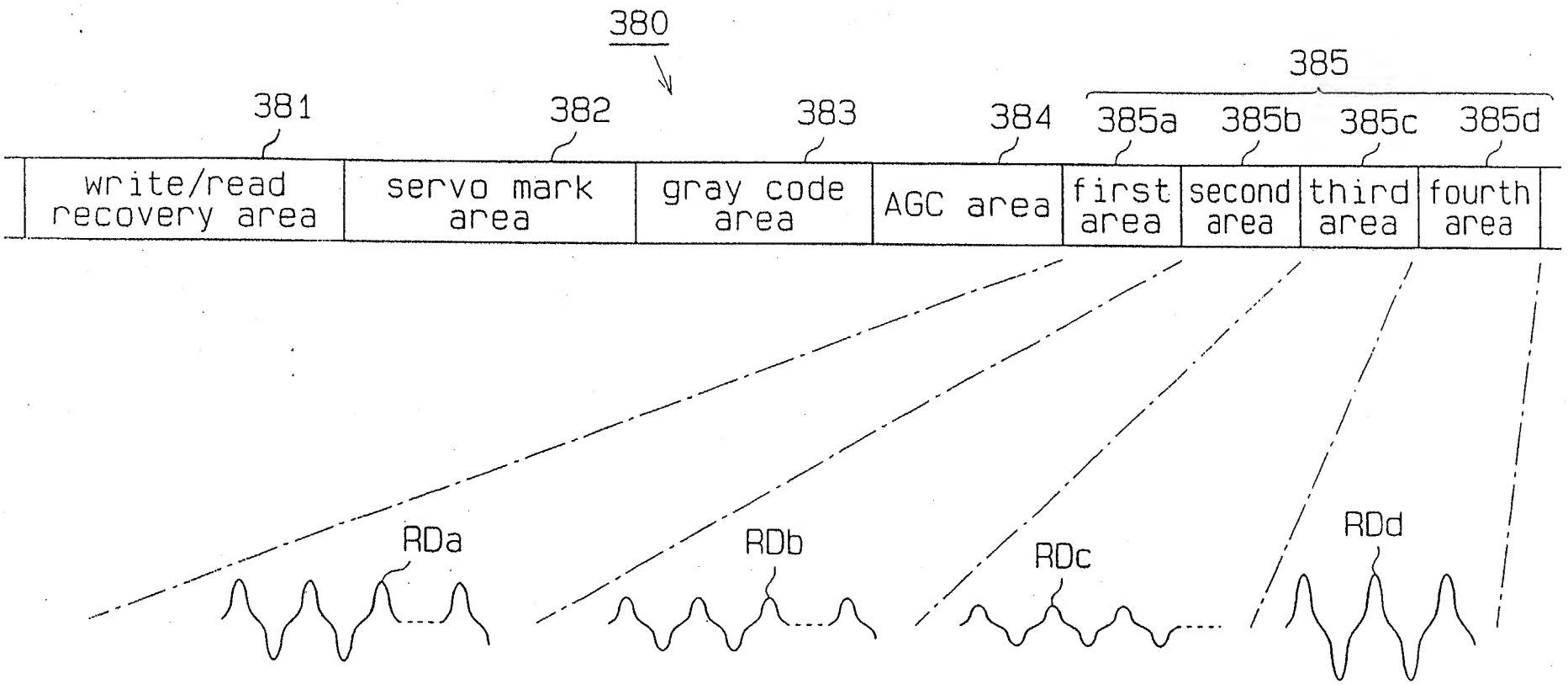


Fig.26

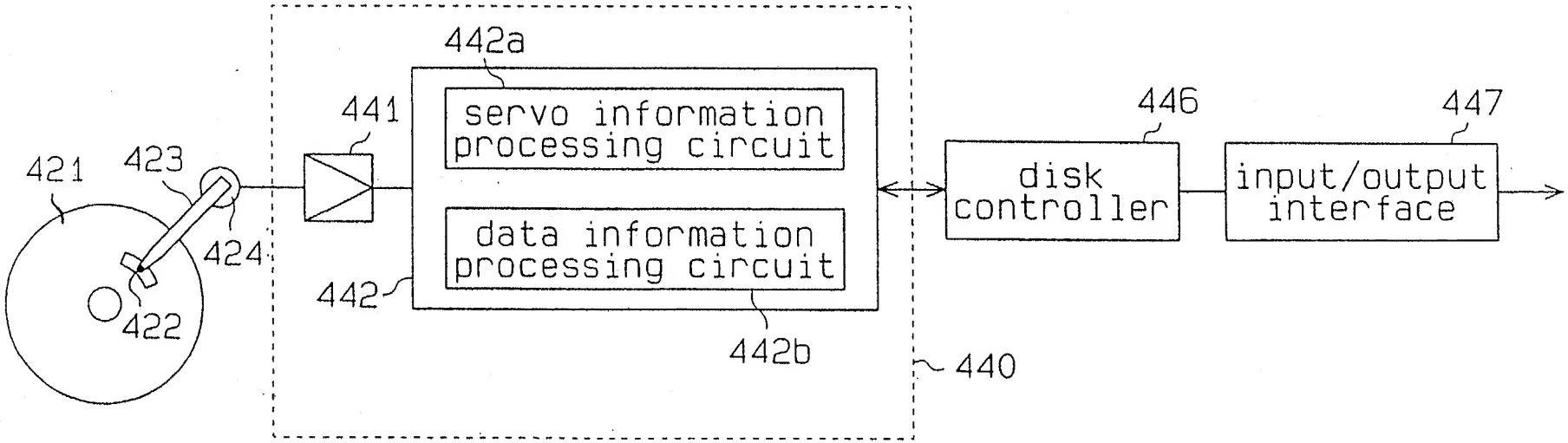


Fig.27

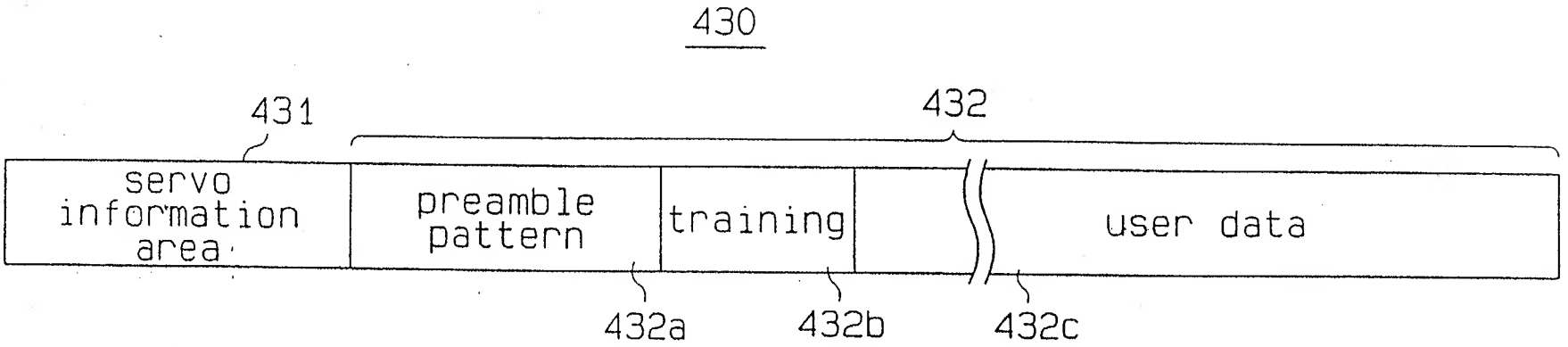


Fig.28

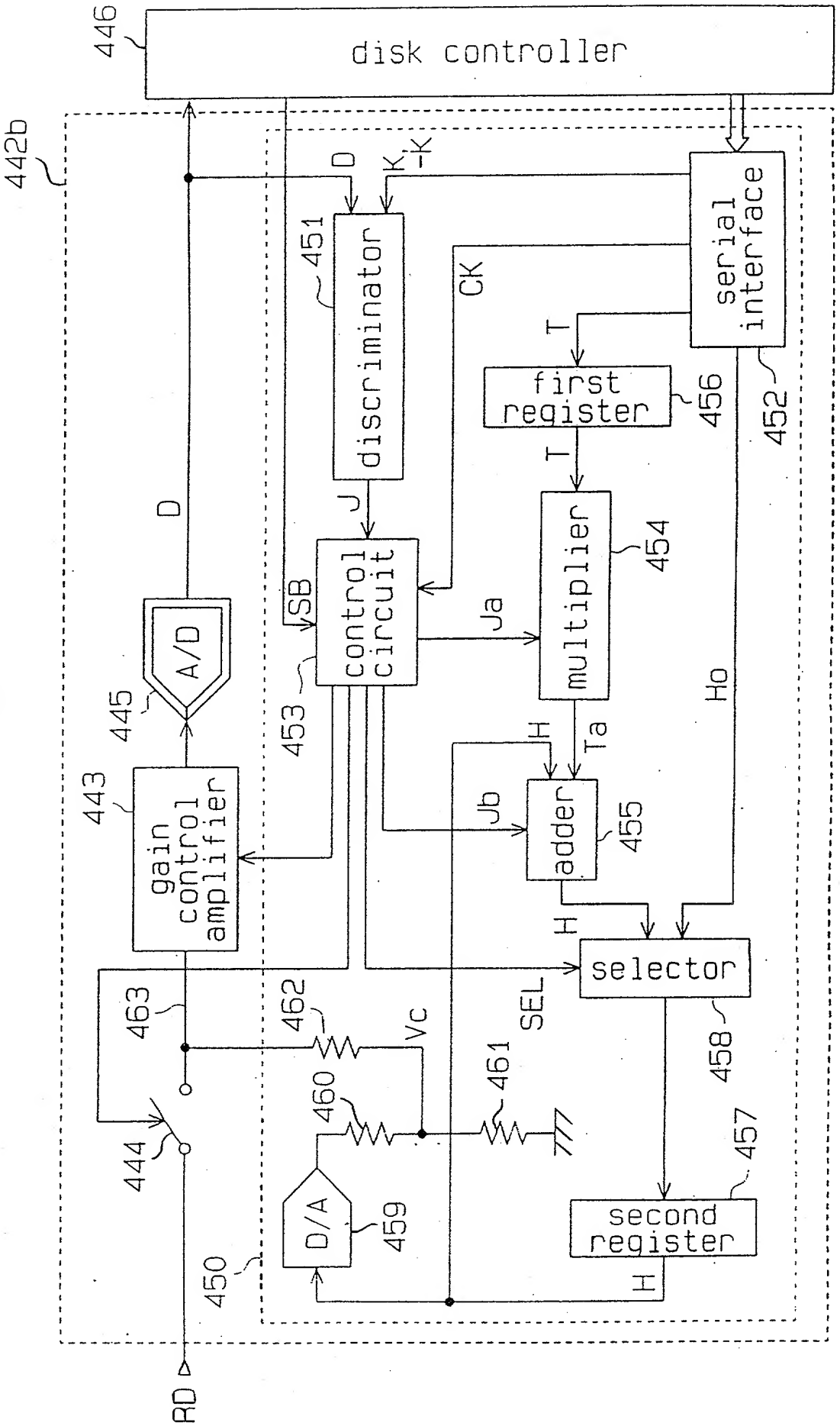

446
disk controller
442b
D
K
-K
451
discriminator
CK
serial interface
T
first register
456
452
T
multiplier
454
J
SB
control circuit
Ja
453
A/D
445
D
H
Ta
Ho
443
gain control amplifier
Jb
adder
455
H
selector
463
462
Vc
SEL
458
461
460
444
D/A
459
457
second register
450
H
RD

Fig.29

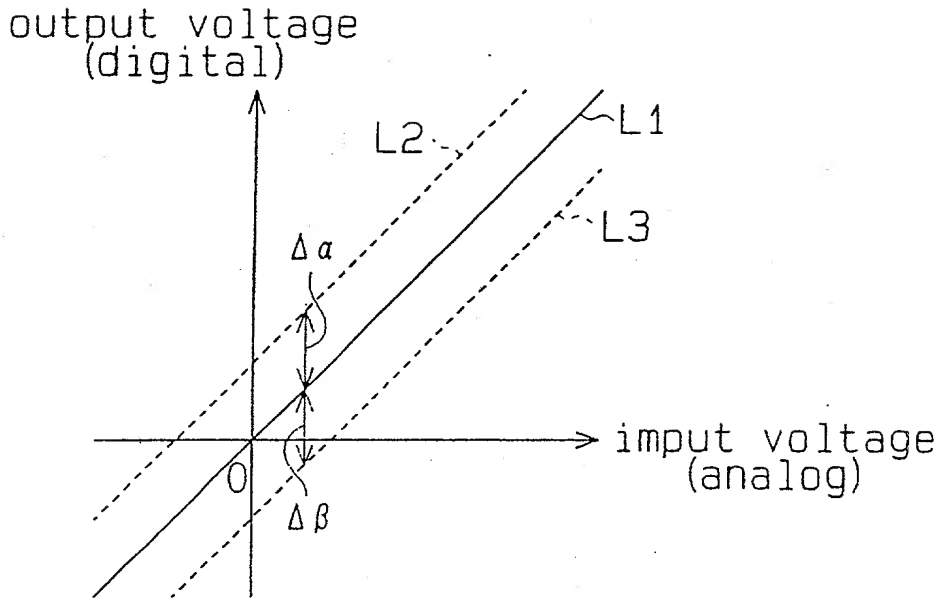


Fig.30

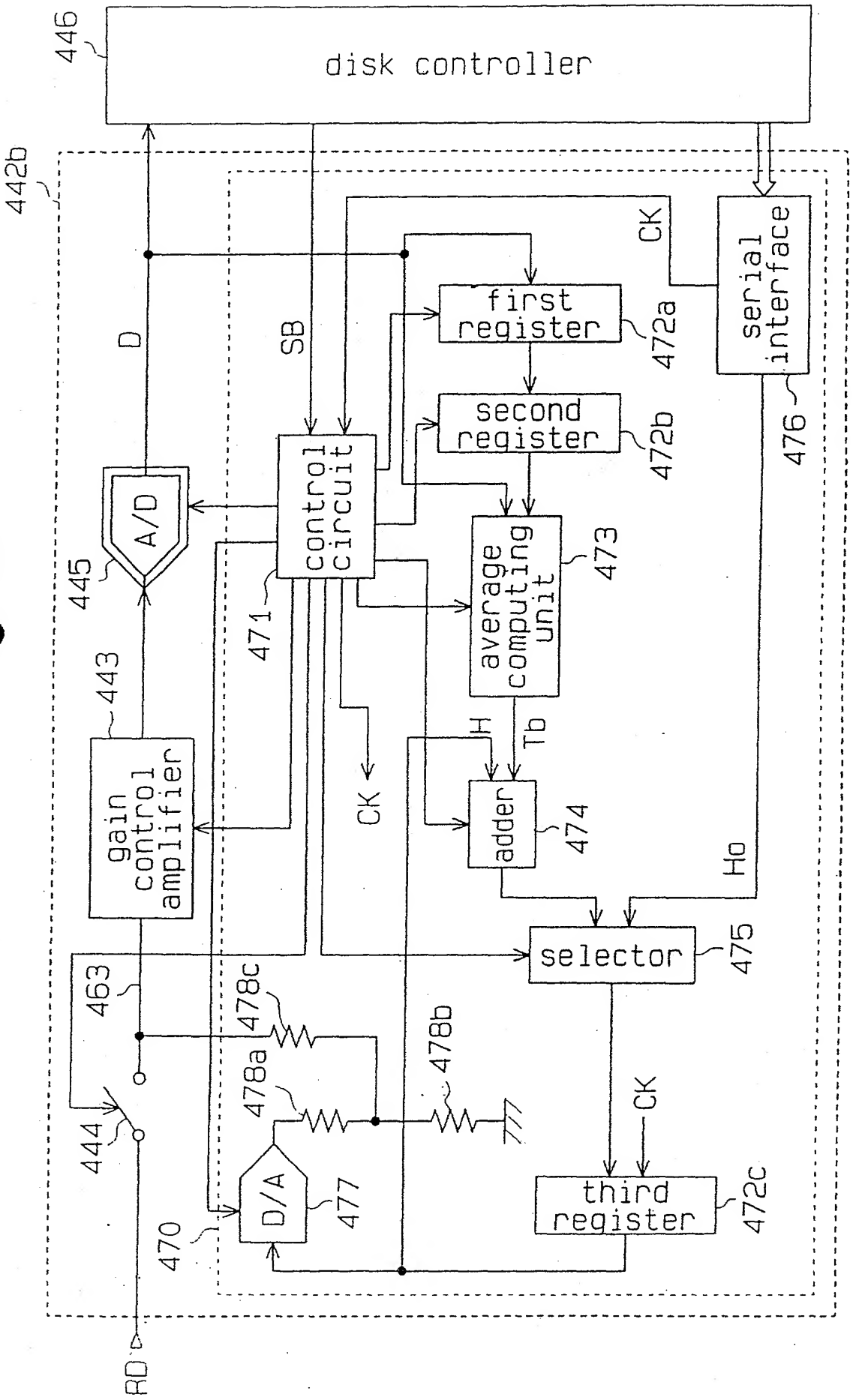

446
disk controller
442b
D
SB
CK
first register
472a
second register
472b
serial interface
476
A/D
445
control circuit
471
average computing unit
473
443
gain control amplifier
H
Tb
CK
adder
474
Ho
selector
475
463
478c
478b
478a
444
D/A
477
470
CK
third register
472c
RD

Fig.31

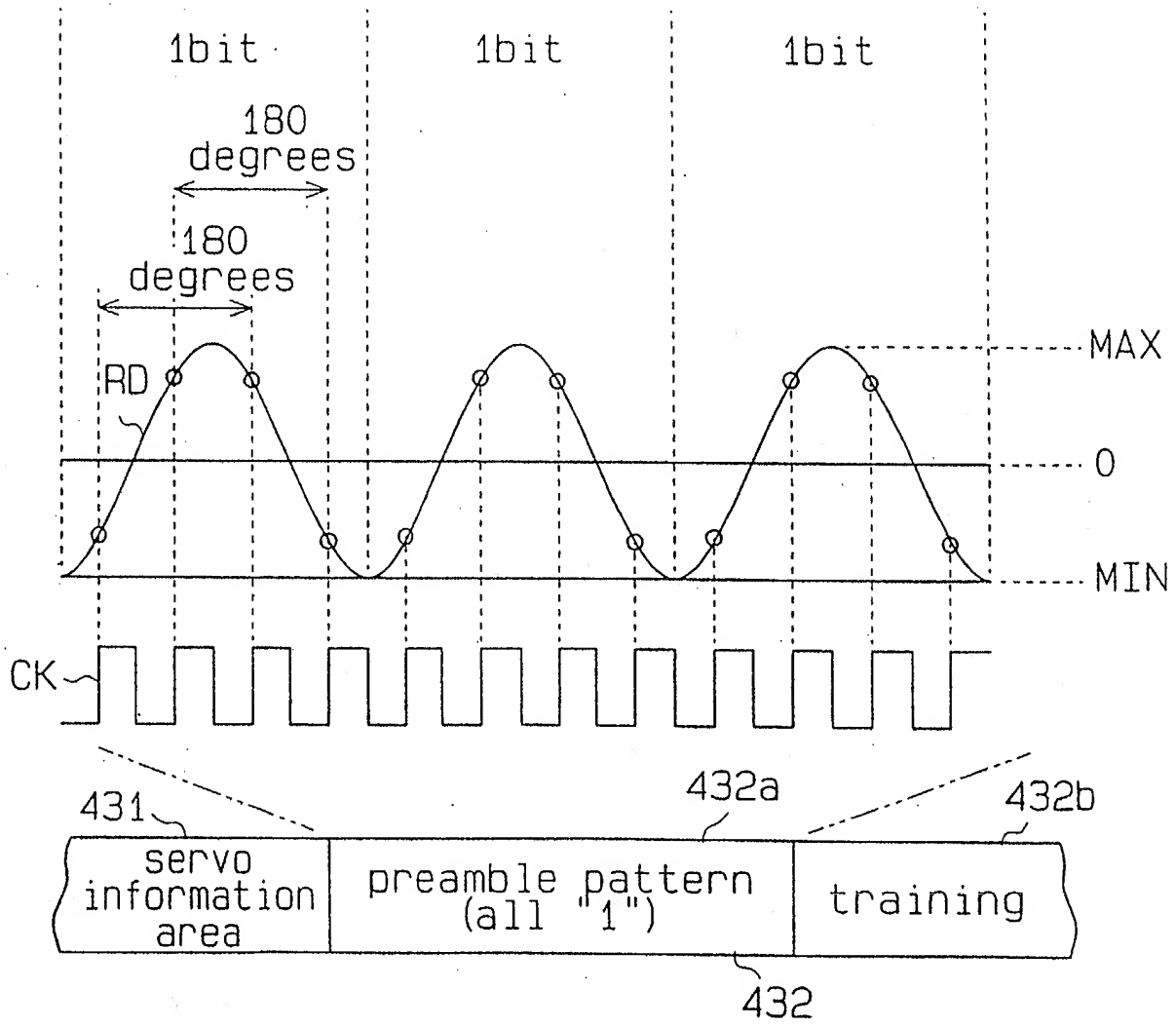


Fig.32

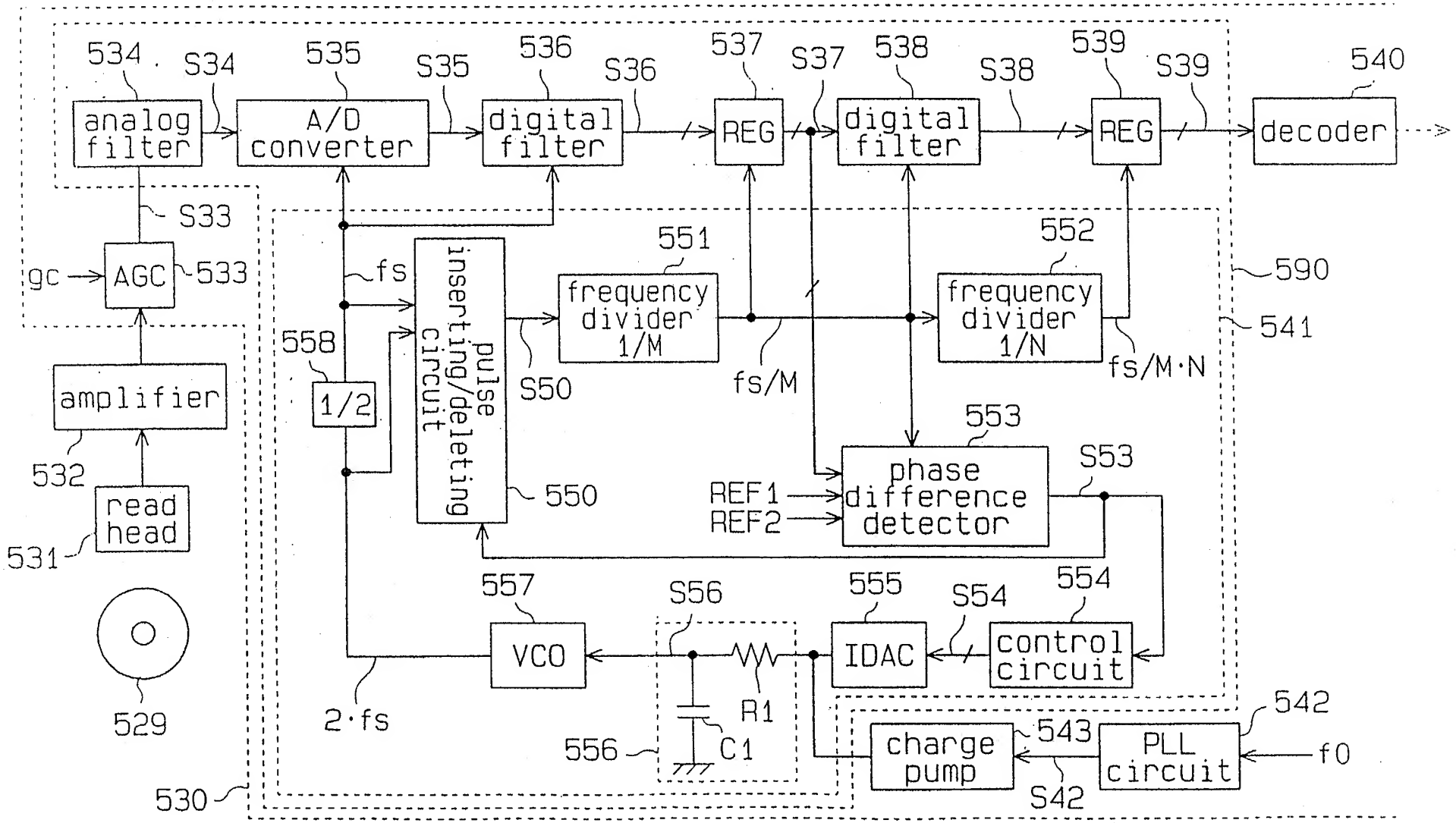


Fig.33

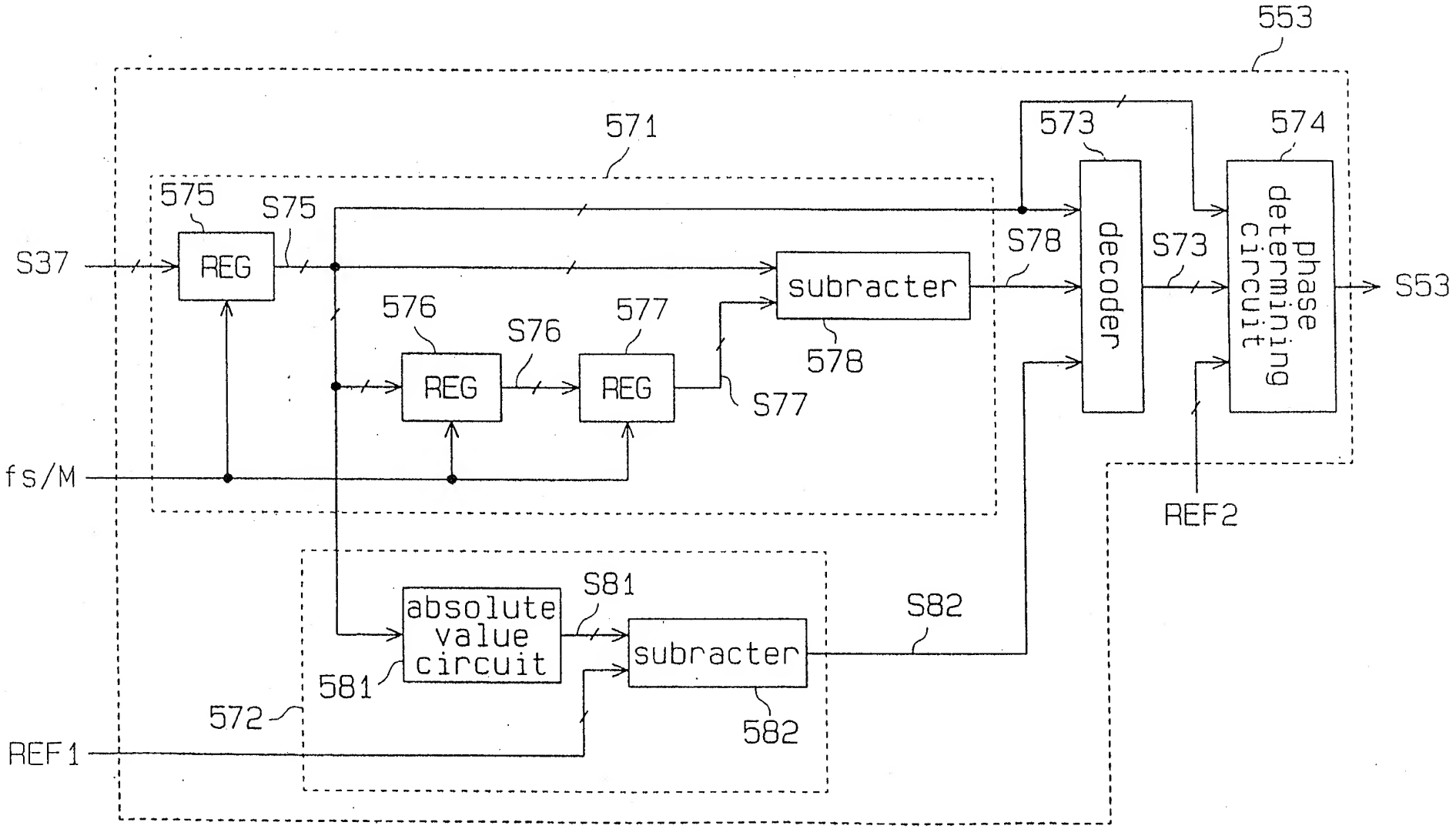

553
571
573
574
575
S75
S37
REG
subracter
S78
decoder
S73
phase determining circuit
S53
576
S76
577
REG
REG
578
S77
fs/M
REF2
S81
absolute value circuit
S82
subracter
581
572
582
REF1

Fig.34A

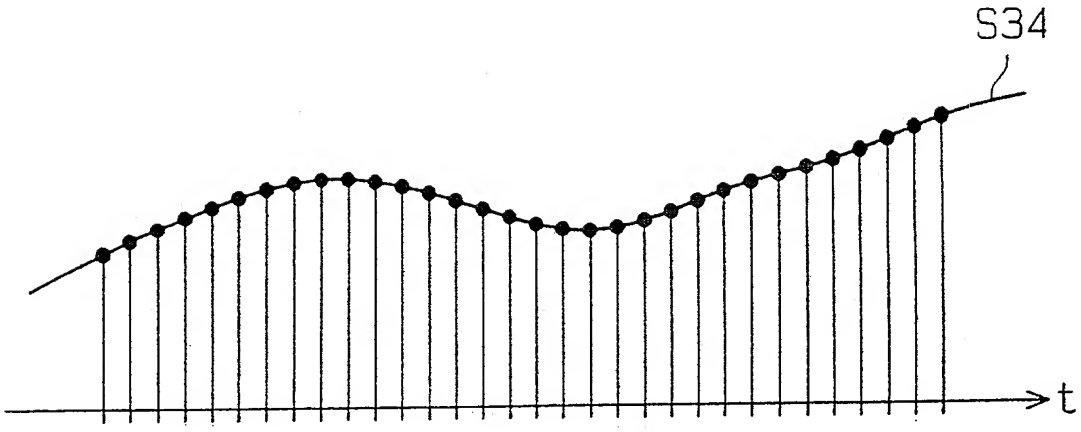


Fig.34B

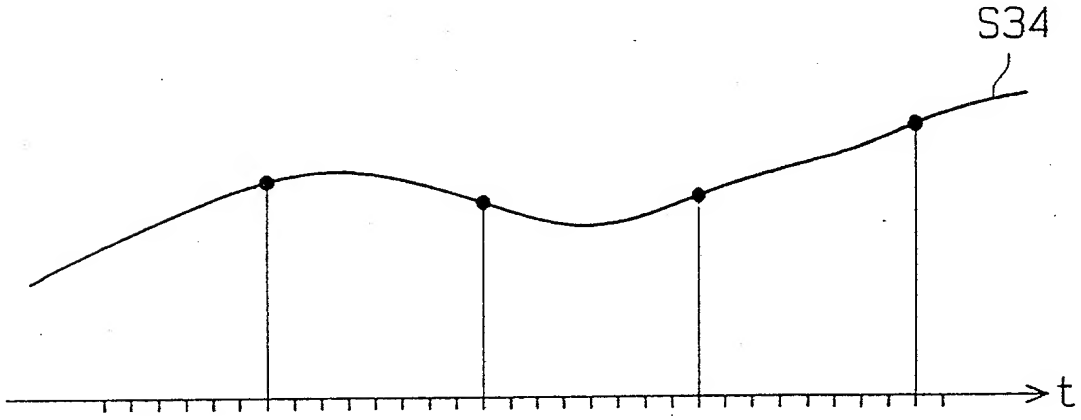


Fig.34C

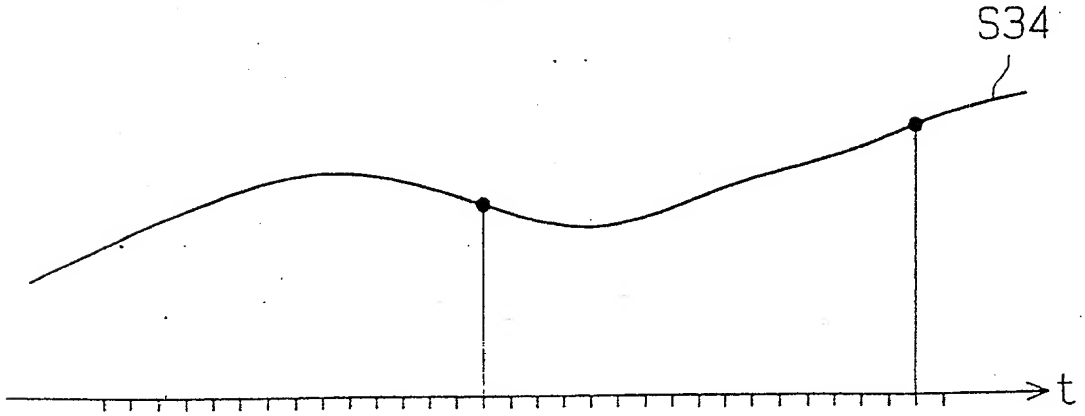


Fig.35

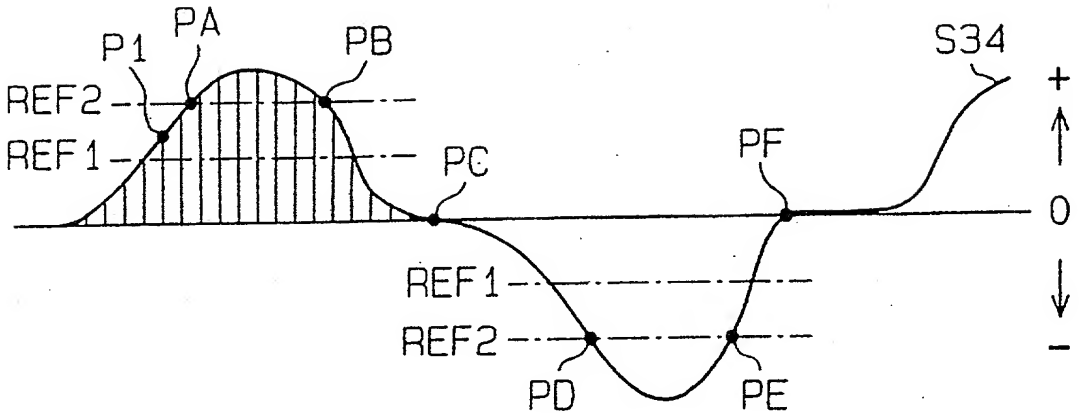


Fig.36

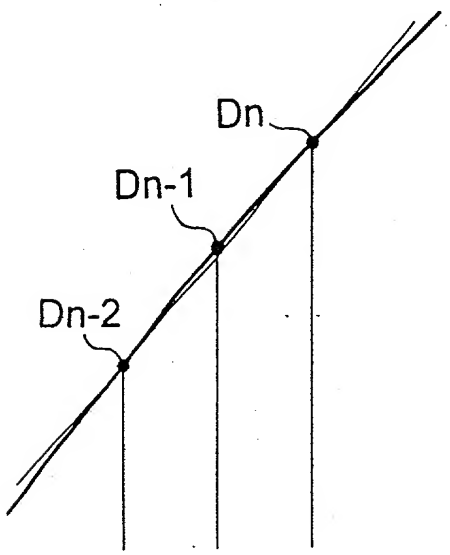


Fig.37

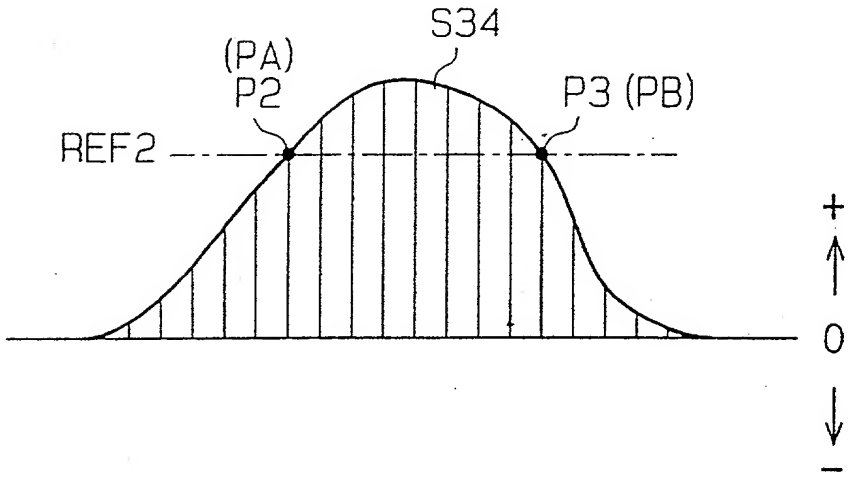


Fig.38

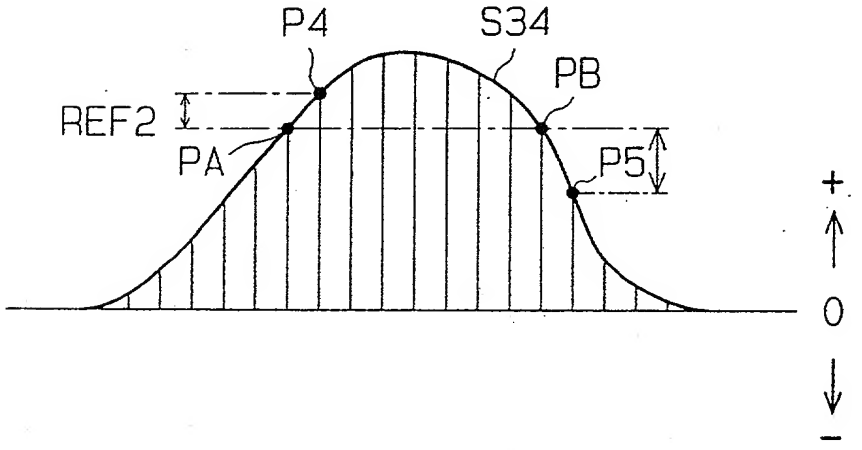


Fig.39

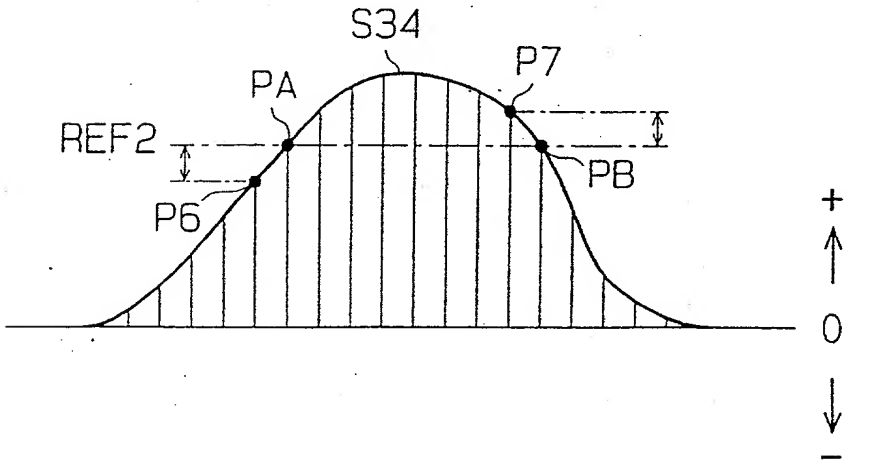


Fig.40A

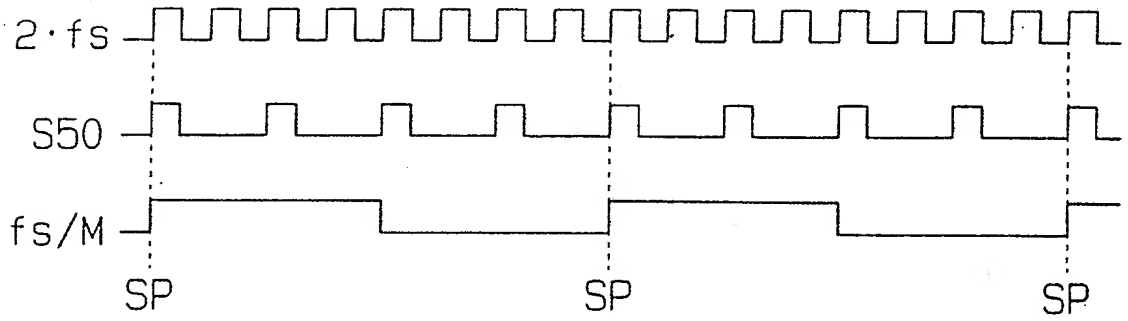


Fig.40B

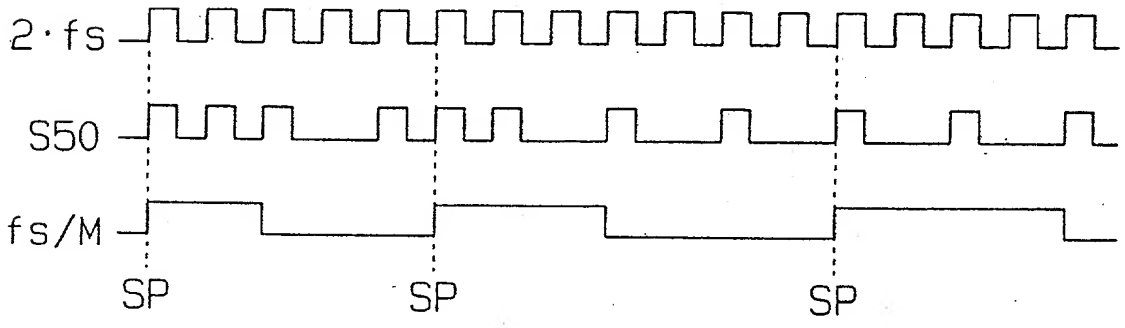


Fig.40C